analog dialogue

A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete

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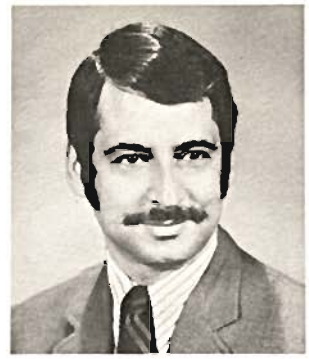
ANALOG DEVICES

Editor's Notes



GETTING TO KNOW YOU

We recently mailed out a questionnaire to a small sample of our mailing list, asking a number of questions. It was our hope that the answers would guide us toward making the *Dialogue* increasingly useful to our readers. The responses, which have just started coming in, are rather informative, and we want to express our appreciation to those of you who have taken the time to respond. We hope to make some of the results known to you in future issues, both in numbers and through improvements that may appear desirable.

One statistic that made an early appearance was that many of the readers who responded have been with us for only one or two years. Since the *Dialogue* is only a year younger than Analog Devices (which celebrates the completion of its first decade in January '76), a reasonable conclusion is that many of our present readers are unfamiliar with many of ADI's contributions during the past decade.

Rather than attempt to cram an array of details into this brief column, we invite any interested readers to catch up by requesting copies of our 1975 *Product Guide*. For an inkling as to our present position and future directions, we invite interested readers to write for our latest Annual and Quarterly Reports and for copies of two technological reports that may be of interest, "Structural Changes and New Opportunities in the Electronics Industry", and "Control Systems in the Continuous-Process Industries".

I.C. CONVERTERS

As the implications of minicomputers and microprocessors became more-widely known and discussed, interest in A/D and D/A converters has produced a great many competitors, with products ranging from large epoxy modules to low-cost IC's, and with talents ranging the gamut from the brightly innovative to the merely imitative.

Through it all, Analog Devices has been the acknowledged leader in converters. Starting with the development of our earliest monolithic quad switches and resistor networks before 1970, we have led in innovation, in quality, in quantity of precision IC's shipped, and in competitive pricing, as well. Now it appears that users of converters, including our present readers, are about to reap the benefits of increasing numbers of successful converter designs in the IC field.

The pace quickened during the past year or two, with the introduction of the 10-bit CMOS AD7520 DAC, the laser-trimmed AD562 and AD563 12-bit DAC's, the 10-bit microprocessor-compatible AD7570 10-bit A/D converter, and, now the AD7522 10-bit monolithic DAC-with-registers. All of these are being delivered in quantities to meet users' needs, and there are many more designs nearing completion. The next few years should prove exciting for converter users and manufacturers!

▶▶▶

Dan Sheingold

THE AUTHORS

Richard Wagner (page 3), Managing Engineer at Analog Devices Semiconductor (ADS), has been aboard since its inception as Nova Devices 6 years ago. He set up the linear IC test facility and developed new automatic-test techniques. He originated the concept and techniques for laser-trimming thin-film resistors on active IC's and applied them to the AD532 Multiplier. His earlier career includes radiation-effects research, and design of digital and analog circuits, hybrid products, and missile-tracking stations. The author of a number of papers, he holds two patents.

Chuck Barker (page 19) is a Project Engineer on the Corporate Staff of Robertshaw Controls, in Richmond, Virginia, and is engaged in microprocessor development. Formerly a design engineer with Industrial Nucleonics and Boeing, he holds BSEE and and MSEE degrees from the Universities of Texas (Austin) and Missouri (Rolla). Chuck is an experienced designer of both analog and digital circuits.

Lewis Counts (page 21) is a Staff Engineer at A.D. Semiconductor, where he is designing IC versions of the multiplier/dividers, rms devices, and other analog circuits for which he was responsible as Manager of Analog Product Engineering at ADI's Modular Instrumentation Division. An S.B. graduate of M.I.T., he has designed a variety of circuits, such as X-band radar receivers, picosecond TDR systems, and low-power spacecraft instrumentation.

Fred Pouliot (page 6) is Manager of Marketing, Analog Modules, in ADI's Modular Instrumentation Division. His photo and brief biography appeared in the last issue of *Dialogue*.

Jerry Whitmore (pages 10 and 20) is Marketing Engineer at Analog Devices Microsystems. His photo and brief biography also appeared in the last issue of *Analog Dialogue*.

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LASER-TRIMMING ON THE WAFER

A Powerful New Tool in Precision-I.C. Manufacture Provides Accurate, Easy-to-Use Circuits at Low Cost

by R. Wagner

Production of useful linear integrated circuits (IC's) has been made practical by the simple fact that congruent circuit elements on a given chip tend to match one another. All modern linear-IC designs exploit this inherent matching between V_{be}'s, resistance values, h_{FE}'s, etc., to obtain produceable circuits capable of meeting today's rather tight offset, linearity, and temperature-coefficient specifications.

However, each new circuit generation taxes the IC-designer's ingenuity more heavily to further improve matching and reduce the sensitivity of circuit designs to absolute parameter variations of 20% to 400%, typical of today's processing technology. Circuit-trimming techniques, commonly used in hybrid- and discrete-circuit manufacturing to improve circuit characteristics and/or yields, have not been available to the manufacturer of monolithic IC's; hence the expression, "cast-in-silicon".

Two years ago, Analog Devices Semiconductor (ADS) pioneered a technique of laser-trimming thin-film resistors deposited directly on active IC chips. This breakthrough permitted individual circuit-characteristics to be tailored prior to capping, thus providing acceptable performance for many applications without the need for external adjustment-potentiometers, while maintaining the simplified assembly and resulting high reliability of proven IC production techniques. This trim technique made possible the AD532* internally-trimmed monolithic multiplier, which, for accuracy within 1–2%, has since made externally-trimmed versions requiring four adjustment pots a thing of the past. It also made differential inputs available.

While this was a significant advance, the need for individual chip-handling prevented full exploitation of the cost-reduction possibilities inherent in automated laser-trimming.

Recently, ADS extended this trim technology to allow functional laser-trimming at the *wafer* stage, simultaneously with the conventional probe-and-ink operations. As a result, significant cost reductions, increased throughput rate, and tighter device specs have been made possible.

A new multiplier-divider, soon to be announced (see schematic in Figure 4), is the first product specifically designed to use this Laser Wafer-Trim (LWT) technique. It will offer tighter specs – at lower cost – than the AD532; and it will also be available in chip form, thanks to the new technique to be described. The technique has also been used in producing the AD510†, a new low-V_{OS} (to 25μV *max*) version of the proven AD504† low-drift operational amplifier.

HOW IT'S DONE

The trim system consists of a conventional step-and-repeat wafer prober, interfaced with a 6-watt YAG laser and galvo-

*For information on the AD532 multiplier-divider, use the reply card.

†Use the reply card for technical data on the AD510 & AD504.

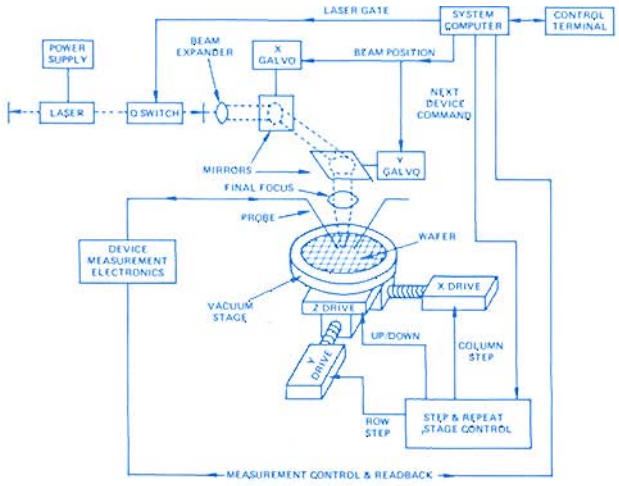

Figure 1. Block diagram of the laser wafer-trim system. The table is indexed by the step-and-repeat mechanism. Further positioning is performed by the use of galvanometer-controlled mirrors that direct the beam along the X- and Y-axes. The galvanometers, in turn, are controlled by the computer.

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beam scanner, all under the control of a digital minicomputer. This adaptation of a Teradyne W311 laser-trim system includes a programmable measurement-electronics package to facilitate completely-automatic measurements of a wide variety of linear IC's under computer control (Figures 1 and 2).

The sequence of operations (see flow chart) starts when an operator loads a wafer on the step-and-repeat stage and rotates it until the chip-rows are aligned with the X and Y axes of the table. Next, the stage is positioned so that the probes align with the bonding pads of the chip, and the height of the probes is set for proper contact pressure. From this time, operation becomes completely automatic.

The stage raises the wafer to contact the probes, then sends a "ready-to-test" signal to the computer. An automatic test sequence is initiated, starting with basic power-supply-current and functional-swing tests, and works its way up to final accuracy, linearity, and offset tests. During these tests, electrical voltages suitable for nulling-out the device errors (to the degree that they can be minimized) are determined and applied. If the chip passes all these tests, the laser-trim program starts.

One by one, the electrical nulls are turned off, and the laser beam is guided to the appropriate resistor for the permanent trim. The beam is gated on and moved until the measurement is satisfied (Figure 3). This sequence continues until all trims are completed.

Finally, another series of tests is performed to grade the device. The laser writes the bin number on a thin-film scratch-pad area for subsequent chip-sorting by quality grade.

If, at any time during the sequence, a test is failed, the device is immediately rejected, and the next chip is stepped into position. This process is repeated until the entire wafer has been probed, as shown in the flow chart. The result: a completely-probed-and-trimmed wafer, with no extra handling, and requiring only a little more time than simple probing.

SMART TRIMS USED

The precision demanded by the new generation of linear IC's requires a departure from conventional trim techniques. For example, the resistor geometries associated with IC's are much smaller than are ordinarily encountered in thick- and thin-film network trimming. This makes placement of the laser beam extremely critical.

To correct for step-and-repeat and initial alignment errors, an edge-sense routine causes the beam to scan (X, then Y) until a pair of orthogonal resistors have been nicked, as evidenced by a resistance change. Once these reference edges have been found, the computer determines the correct placement of all the other trims.

Trim speed is primarily limited by the measurement intervals. Therefore, for trims requiring large value-changes, a measure-predict mode is used: the length of trim to achieve 90% of the final value is predicted, based on a single measurement. The cut is made, and a new measure-predict cycle occurs, repeating until the final value is within tolerance.

Special proprietary trim techniques had to be developed to achieve sufficient range and resolution without a severe

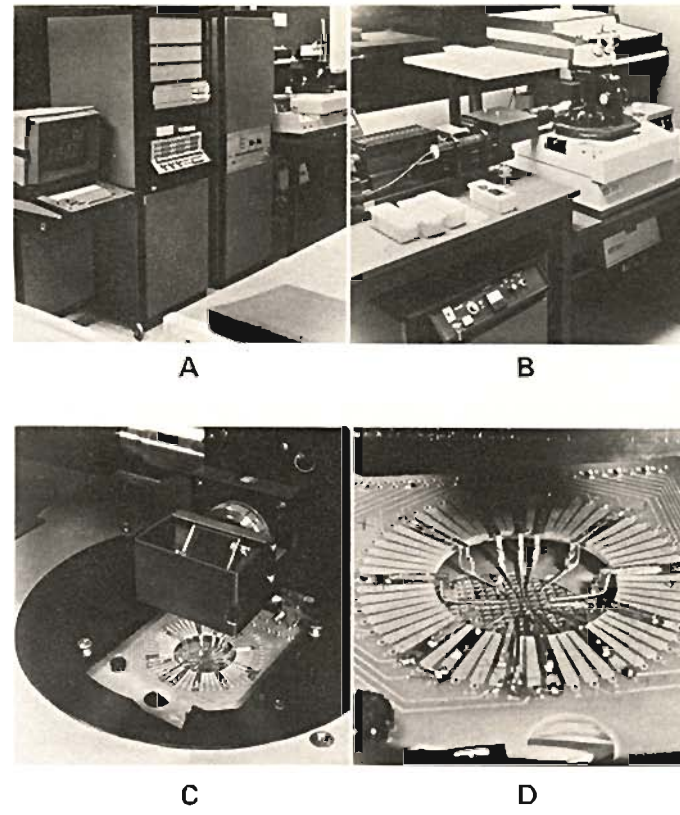
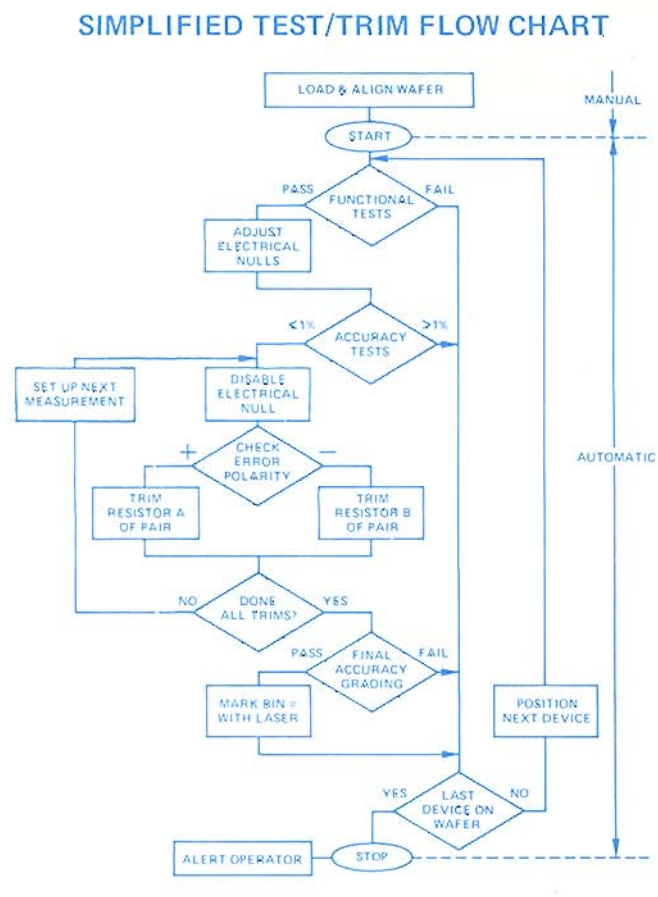


Figure 2. Photographs of the system. (A) shows the entire system. (B) shows the step-and-repeat table, the laser, and its control electronics. (C) is a closeup of the table and the beam-deflection box. (D) shows the wafer and probes in position on the table.



resistor-size penalty. This is particularly important, because the ultimate wafer yield bears a strong inverse relationship to chip size.

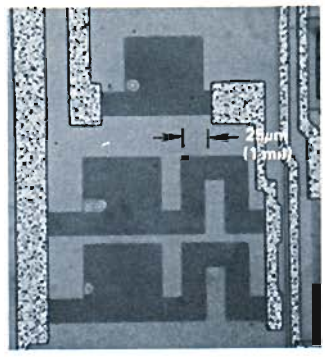


Figure 3. Some of the resistors after trimming.

HOT BUT COLD

It takes a temperature greater than 1200°C to cleanly vaporize the thin-film resistor material used at ADS; yet temperature differentials of 0.05°C between critical devices on a chip may cause significant measurement errors! This apparent paradox is resolved in practice by careful circuit layout, processing, and laser adjustment.

Where possible, resistors-to-be-trimmed are positioned on the thermal centerline between devices which must match during the associated trim. In this way, the differential temperature seen by the devices is balanced out despite some heating during the trim.

The thin-film resistors are deposited on a relatively thick oxide, which provides a high thermal resistance to the silicon substrate containing the active devices. The mass of the resistance layer under the laser is extremely small, which minimizes the laser energy needed to vaporize the material. On the other hand, the Si substrate, having a relatively large mass, high specific heat, and good thermal contact to its supporting stage, dissipates the laser heat quite efficiently, minimizing device heating.

OPTICAL CONSIDERATIONS

Stray laser light can cause measurement errors by inducing photocurrents in various semiconductor junctions, which behave like photodiodes in infrared. However, by strobing the measurements to occur *between* the laser pulses, this effect is minimized. Locating sensitive devices away from the trim area avoids possible device saturation by excessive photocurrents, with the consequent slow recovery.

Efficient coupling of the laser energy to the thin-film resistors is dependent on many things, such as oxide thickness, passivation thickness and doping, substrate doping, resistor density, etc. Though all these parameters are relatively constant across a wafer, wide variations occur from lot to lot. A proprietary monitoring technique controls laser cut quality to prevent trim instability due to incomplete film vaporization or structural damage – very important in a high-volume trim operation.

FUTURE OUTLOOK

From the user's point of view, laser wafer-trim has many significant advantages, beginning with lower device cost and tighter specs. Additional cost savings will be realized in terms of reduced labor-and-material cost through the elimination of various external null- and gain-adjustment pots. That this is important is shown by our experience in the marketplace with the AD532 multiplier-divider. Though it is more costly and has somewhat more-modest performance specs than its predecessor the AD530 (after the AD530 has been trimmed), the internally-trimmed AD532 is the overwhelming choice of users.

Now, with the advent of LWT, the new multiplier (Figure 4) will give the user even tighter specs, with concurrently lower cost.

Many new IC products, currently under development at ADS, using laser wafer-trim and related techniques, can be expected to accelerate the encroachment of monolithic circuits on performance areas hitherto served almost exclusively by discrete modules and hybrids.

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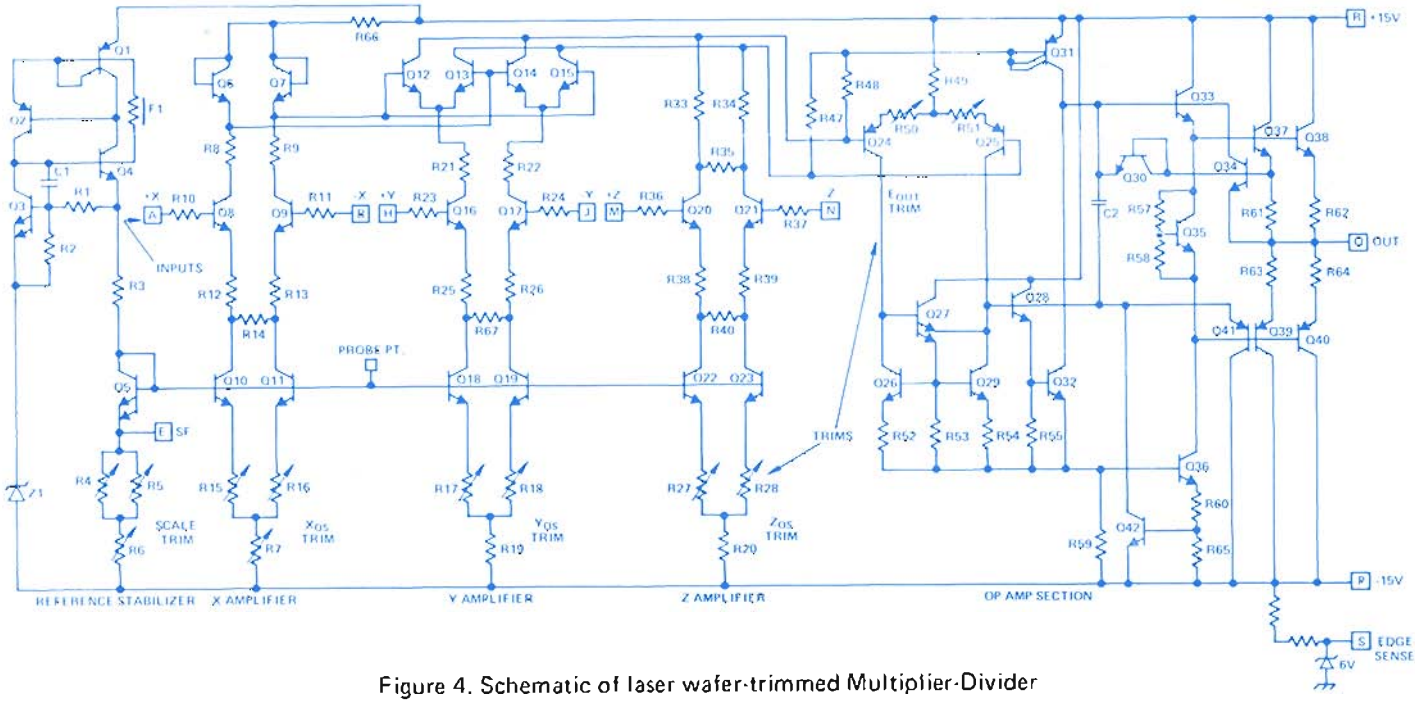


Figure 4. Schematic of laser wafer-trimmed Multiplier-Divider

HAVE YOU CONSIDERED V/f CONVERTERS?

They Offer High Resolution at Low Cost
Use Them for Digitizing, Isolating, Integrating, and Much More

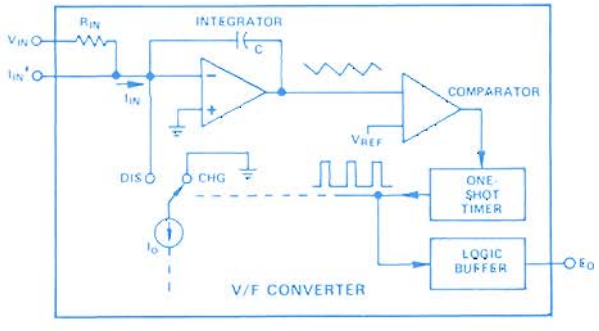
by Fred Pouliot

Voltage-to-frequency converters are now available as small, economical modules characterized by high resolution, low nonlinearity, and excellent temperature-stability.* In many data-handling applications, they have proved to be an excellent alternative to both analog and digital techniques.

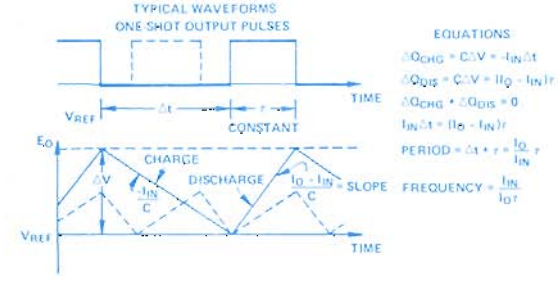
Voltage-to-frequency converters, of the kind to be discussed, are signal-processing devices that accept an analog input and convert it to a train of pulses having fixed width, fixed height, and a rate that is directly proportional to the input voltage or current. For an arbitrary voltage input, $0 \leqslant V_{IN} \leqslant V_{MAX}$, and a corresponding full-scale frequency, f_{MAX}, the frequency of the output pulse train, f, is

$$f = f_{MAX} \frac{V_{IN}}{V_{MAX}} \qquad (1)$$

V_{MAX} is usually 10V, often with 50% overrange capability. The relationship between analog input and the output frequency is inherently monotonic, making it possible to construct V/f-based analog-to-digital converters of extremely high resolution, exhibiting no missing codes, even in the presence of widely-varying ambient temperature. Noise rejection is inherently quite high, first because of the internal integrator, and second – in cases where the output is counted – because of the integrating effect of the count.



(a) Block Diagram



(b) Waveforms and Equation. Dashed line shows waveforms for doubled input (near I_{MAX}, f_{MAX})

Figure 1. A Charge-Balance V/F Converter

*For data on V/f converters from Analog Devices, use the reply card.

HOW IT WORKS

Figure 1a is a block diagram of a V/f converter of the *charge-balance* type, a modern form of conversion that results in high linearity and stable performance. The input current – whether furnished directly to the summing point or determined by the input voltage and R_{IN} – flows at all times through the feedback capacitor, C, tending to charge the capacitor at the rate $-I_{IN}/C$, proportional to the input. During the *charging* portion of the cycle, a precisely-determined current, I_O, somewhat larger than I_{MAX}, and opposite in polarity to I_{IN}, is steered to ground.

When the output of the integrator reaches the internal reference voltage, V_{REF}, the crossing trips a comparator, which initiates a pulse of fixed amplitude and precise duration, from a one-shot timer. This pulse is buffered and transmitted to the output. The timer also operates a switch that steers the current I_O to the summing-point of the integrator, discharging it linearly for the pulse duration, τ, at a rate $(I_O - I_{IN})/C$.

At the conclusion of interval τ, I_O is switched to ground again, and C is once more charged by I_{IN}.

If I_{IN} is constant, the amount of charge $(I_{IN}\Delta t)$ acquired during charging is equal to the amount discharged $(I_O - I_{IN})\tau$, and the equations in Figure 1b show that the pulse frequency is

$$f = \frac{I_{IN}}{I_O \tau} \qquad (2)$$

When the input level, I_{IN}, changes, the integrator immediately changes to the correct rate; the period starting with the next discharge cycle will be accurately determined. For typical commercially-available devices, with f_{MAX} = 10kHz, τ is somewhat less than 100μs; I_{MAX} is usually about 0.5mA, equivalent to 10V in 20kΩ. When used with a counter, the resolution depends on the counting period; a device with a maximum frequency of 10^5Hz will have ten times the resolution of a 10^4Hz device, or 10X faster response at the same resolution.

LONG-TERM INTEGRATION WITH V/f's

Voltage-to-frequency converters are rapidly replacing purely-analog circuitry in applications requiring long-term integration. Conventional integrators use a high-quality capacitor and an amplifier selected for low drift and negligible bias current. With the use of high-quality components and considerable care, integration times of several minutes, or even an hour, can be realized with accuracy to within 0.1%. Eventually, errors due to dielectric absorption, leakage, finite open-loop gain, bias current, and drift limit the accuracy; and finally, over a long-enough period, the amplifier simply runs out of output range and drifts into limits. For integration periods of one hour with accuracy to within 0.1%, the cost of the capacitor becomes prohibitive, since a leakage rating of 3.6×10^6 megohm-microfarads is required.

The V/f converter, when combined with a low-cost counter, as shown in Figure 2, offers both improved accuracy and virtually unlimited integration time, with an overall reduction in system cost. To accomplish integration with a V/f converter, one needs only to apply an input voltage, then count the output pulses. The accumulated count is proportional to the integral of V_{IN} over any arbitrarily-chosen period, and is limited only by counter capacity.

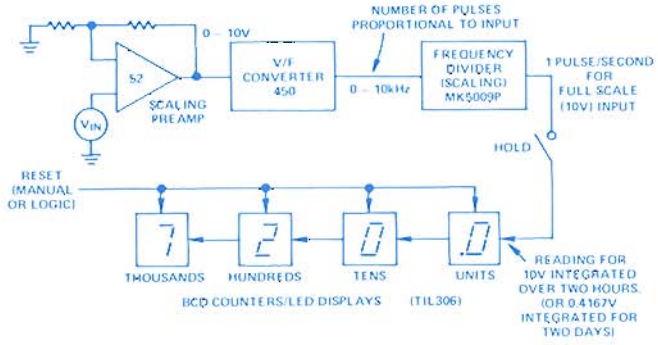


Figure 2. V/F converter as a long-term integrator with arbitrary display calibration. Frequency division ratio can otherwise be chosen to provide direct readout in any desired units.

The system shown in Figure 2 displays, in numeric form, the integral, over an arbitrary time interval, of an analog voltage. It is based on a 10kHz VFC, Model 450, from Analog Devices. The input voltage, V_{IN}, is amplified by a high-accuracy, low-noise op amp (Model 52), which provides 10V full scale to the converter input. The 10kHz-full-scale output pulse train of the VFC is applied to the input of an MOS counter-time-base circuit, MK5009P, used as a frequency divider with a division ratio of 10,000:1. The output of the divider produces one pulse/second for full-scale input. These pulses increment decade counters-and-displays, TIL306. With 10V constant input, the displayed digits are a direct representation of the integration time in seconds and may be used for calibration. The count continues until a manual or logic command places the counter in *hold* by disconnecting its input, or resets the count.

With input of +10V, 9999 seconds are required to produce a displayed reading of 9999. With less input voltage, proportionally more time will be required to fill the counter, or, if the counter is allowed to count for the same time period, it will display a proportionally smaller value before being reset.

V/f converters as long-term integrators of analog signals are practical and useful, but there are some limitations. The effect of drift on the accuracy of integration of *unipolar* signals is simply related to the ratio of the input offset to full-scale input. For example, if the offset is 10μV, and full-scale input is 10V, drift error will always be 1ppm of full-scale; if the *average* input signal is 10mV, the drift error will be only 0.1%, no matter how long the integration continues, as long as sufficient counter capacity has been provided. If the converter is used as an integrator in a control loop, with input variations of ±5V about a +5V set point, input offsets will result in small "position" errors of the fed back signal.

A/D CONVERSION WITH VFC's (Figure 3)

A VFC continuously tracks the input signal without the need for clock pulses, convert-command signals, or any form of external control logic. The direct count of its output pulses, over a time period (vs. measurement of its frequency by discrimination techniques, phase-locked loops, etc.) produces a binary or BCD (binary-coded decimal) digital number, which represents the average value of the input during the counting period. The VFC pulses require but a single wire-pair for transmission, unlike parallel converters, which, for n bits, require n + 1 wires, or serial converters, which require some form of synchronization. Of course, the V/f converter is much slower;

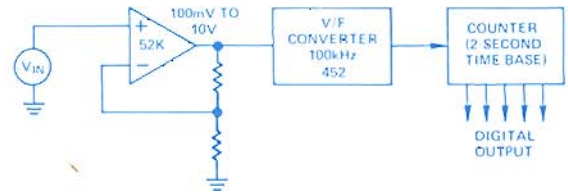


Figure 3. V/F converter used as a nearly 18-bit binary (5½BCD) A/D converter. Resolution is 1 pulse in 200,000, or 0.05% of smallest input signal (or 5ppm of full scale).

even a 100kHz converter still requires 4096 counts (41ms) for 12-bit resolution. Though the VFC continuously tracks the input, it differs substantially from the tracking up-down counter-comparator type of converter, in requiring only a single wire-pair for communication. Furthermore, it is all but unaffected by spike-type errors, since their effect, at worst, is generally limited to one count.

Readily-Adjustable Scaling for Faster Conversion Rates

When using V/f converters in analog-to-digital conversion, in applications where system resolution requirements permit, it is often advantageous to offset and rescale the input for the sake of faster conversion rates. Such may be the case when data is to be transmitted or recorded. To accomplish the offsetting, a current is applied to the appropriate V/f input. For Model 452, a 100kHz VFC, full-scale is normally obtained with a 10V input. If an offset current of 0.05mA (equivalent to 1V in, or 10% of normal full scale) is applied to the current input, the new full scale range will be from 110kHz for 10V input to 10kHz for 0V input instead of 100kHz to 0 (most VFC's have sufficient overrange tolerance to handle the increased full-scale output accurately).

The improvement in conversion speed is evident. Without the offset, minimum conversion time is 10ms to guarantee the occurrence of a single pulse, for a 10mV input; with the offset, one output pulse will occur every 100μs for zero input, and every 99μs for 10mV (10.1kHz).

Bipolar signals with 20V peak-to-peak range can be converted by adding an offset equal to one-half the full-scale range. When counted by a binary counter, the digital output will be *offset-binary*-coded (identical to 2's complement with the most-significant bit complemented). For model 454, a 0.33mA offset would allow a 0 to 10kHz output to correspond to a ±10V input range.

The easy adjustability of output count, by using frequency division or an arbitrary time base, allows the digital output number to directly reflect engineering units, representing flow rate, force, pressure, or other transducer inputs.

EXCELLENT RESOLUTION AT LOW COST

An inexpensive 10kHz VFC offers resolution of 1 part in 10^4 when integrating over a 1-second period. This exceeds the resolution available in a 13-bit A/D converter (1 part in 8192). Nonlinearity is typically 0.005% (model 450J), which is comparable to that of a 13-bit ADC. Unlike successive-approximation converters, differential linearity to within 0.01LSB is readily obtained at this resolution and is maintained despite wide temperature excursions. Therefore, a low-cost 10kHz V/f converter compares most favorably in linearity and resolution to that of a 13-bit ADC. The comparison becomes considerably more dramatic when a 100kHz converter (model 452) is used over a time base greater than 1 second.

Figure 3 shows how resolution of 0.05% of the *smallest* input signal can be accomplished for a signal spanning two decades. Expressed differently, the resolution here is an amazing 0.0005% (5ppm) of full scale! At the lowest input level, 100mV, 0.05% represents 50μV. The stability of the VFC is consistent with this requirement; the number of output pulses differs by no more than one count when counted during successive 2-second intervals.

HIGH NOISE REJECTION

Unlike successive-approximation or tracking-type A/D's, which can give completely erroneous output codes for large spike inputs, the VFC inherently has high noise rejection.

The output pulse train is counted over relatively-long periods. Noise that appears as a repetitive waveform is averaged out completely over the measuring interval, except for fractional cycles. For example, if the interfering signal is a 60Hz sine-wave, the worst-case contribution to the output, which occurs when the measuring interval is one-half cycle too short or too long, is 1/120 of the ½-cycle average, when the measuring interval is in the vicinity of 1 second.

If the count time is an integral multiple of the line period, rejection is theoretically infinite — and better than 80dB in practice. Since the counting period for V/f converters is determined externally, it can be set to provide maximum rejection for the most-troublesome noise frequencies. For example, multiples of a counting period of 0.1Hz will reject line frequencies of 50 or 60Hz. And if the fundamental has an integral number of cycles during the counting period, and is therefore strongly rejected, the harmonics will also be rejected.

LIMITATIONS OF V/f CONVERTERS

In the face of their many advantages, there are only two significant drawbacks to their increased usage in data transmission:

1. They are slow in converting small signals.
2. They require a device, such as a counter, to interpret the output digitally, or an integrator (or f/V converter) for analog readout (where the purpose of conversion was to transmit the analog signals through a noisy environment).

The speed of conversion of a VFC is determined by the full-scale count and the amplitude of the signal being measured:

$$\text{Conversion time} = \frac{\text{Desired full-scale count}}{\text{Max. input to be measured}} \cdot \frac{\text{Unit's F.S. input}}{\text{Unit's max. frequency}}$$

For example, if a 10kHz VFC is to be used to measure inputs from 0 to 2.5V with resolution of 1 part in 1000, the conversion time is (1000/2.5) (10V/10kHz) = 0.4 seconds, minimum.

To improve the speed, here are two reasonable solutions: First, a higher-resolution converter, such as the 100kHz Model 452, could be used to decrease conversion time by a factor of ten. Second, using the current input, one could select an external scaling resistor such that the full-scale input current (normally 500μA) is realized when 2.5V are applied, which will further reduce conversion time by a factor of 4. In this example, a 5kΩ external resistor would be used.

For digital applications, the need for an external counter at the receiving end can be fulfilled at very low cost. There are several low-cost counters available in IC form. For example, the SN7490 BCD counter and the SN7493 binary counter are available in the U.S. at less than $1 each in reasonable quantity. For under $5, a counter with latches, drives, and displays is available, the TIL306.

MORE APPLICATIONS

The most popular applications for V/f converters are those shown in Figures 2 and 3, the long-term integrator and the quantizing element of an A/D converter. There are many other applications where the great flexibility and ease of use of the VFC make it an excellent solution for design problems. Here are a few examples.

Figure 4 shows a digital thermometer, based on the ~(-2mV/°C) change of forward drop of a diode with temperature. For good repeatability and accuracy, a silicon transistor, connected as a diode, is inserted into the probe, forming a reasonably small and convenient sensing element. Back at the instrumentation circuit, transistor Q_1 and its associated components form a constant-current source for the temperature-sensing element, Q_2. An offset current is applied to the VFC by R1, R2, R3 to fix one end of the range, so that direct readout in °C may be obtained. For a display of the temperature range from 0° to 100°C to three significant digits (i.e., with a resolution of 0.1°C), the number of pulses accumulated during the measurement interval must increase by one for a temperature increase of 0.1°C. Each degree C represents a change of 1mV at the converter input, for which the output will change by 10 counts per second. A 1s time base gives a sensitivity of 10 pulses/s/°C.

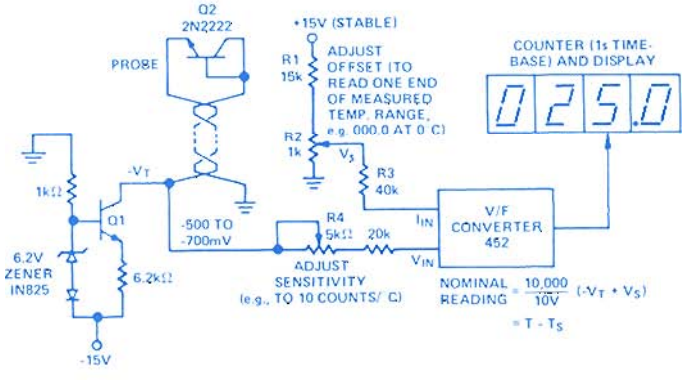


Figure 4. V/F converter as digital thermometer with 0.1°C resolution.

The instrument is calibrated by placing the sensor in ice water and adjusting the offset control until some reading greater than

zero appears. The sensor is then placed in boiling water, and the span is adjusted until the reading is 100.0 (corrected for altitude) greater than for ice. The sensor is returned to the ice bath, and the span is readjusted if the difference is no longer "100.0"; this process is iterated until the difference is "100.0" exactly. If necessary, the offset should be readjusted during this process to maintain the minimum reading greater than zero. The last step, when the span is correct, is to adjust the offset for a reading of 00.0 when measuring the ice bath.

Figure 5 shows a means of using V/f converters to obtain accurate ratio measurements at high resolution. This scheme is an excellent alternative to analog dividers, such as the 434*. Accuracy to within 0.1% can be obtained for signals spanning a range greater than 1000:1.

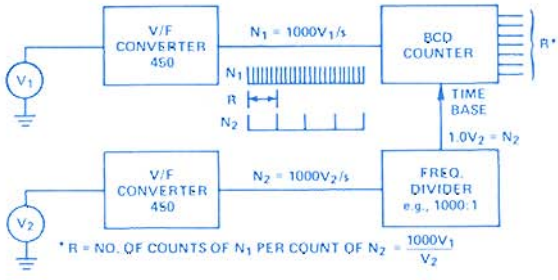


Figure 5. Wide-Range ratiometer (divider of voltages).

A pulse rate proportional to V_1 is applied to the counter's input. The counter is gated for intervals proportional to the period between pulses that occur at a rate proportional to V_2. The total count in each such period is proportional to the ratio of the number of pulses of V_1 to one pulse of V_2, hence the ratio of V_1 to V_2. The frequency-divider ratio is chosen for the required resolution for the specified dynamic range in the shortest time. For best accuracy, (or in low-level applications requiring common-mode rejection), instrumentation pre-amps (see page 23) may be used ahead of the VFC's.

A somewhat similar technique may be used to obtain the fastest possible response from a VFC with a given resolution, at any input level. Since all the information, for a given input voltage, is contained in the time for a single period, each period of the VFC is used to gate a train of pulses at an accurately-known high rate into a counter; at the beginning of the next period, the counted number is strobed into a set of latches, the counter is reset, and another cycle begins. Thus, the output of the latches continuously reads the period of the last pulse-pair, which is accurately proportional to $1/V_{IN}$.

If the reciprocal of V_{IN} is undesired, it can be easily dealt with in subsequent steps of digital computation, or by the use of a read-only memory programmed for reciprocation.

Figure 6 shows an optical-isolation circuit that uses V/f conversion, for accuracy to within 0.1% and a common-mode capability greater than 1500V. The output pulses from a VFC are transmitted via an optical coupler and are then counted on the low-voltage side of the circuit. CMV is limited only by the characteristics of the optical coupler and the power-supply used for the VFC.

As shown in Figure 6, the output is digital, as provided by a counter. If an analog output is needed, a frequency-to-voltage converter can be used at the output of the photocoupler to recreate the input analog signal with appropriate isolation.

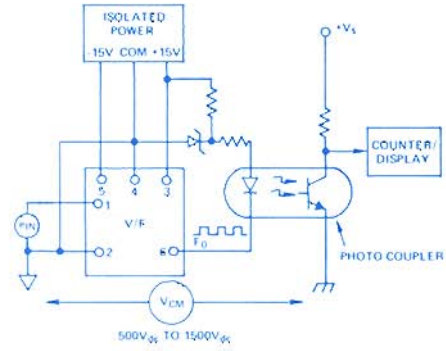


Figure 6. Optically-Isolated A-D conversion.

MORE APPLICATION IDEAS

The range of applications for VFC's is by no means limited to the few examples discussed here. V/f's are also useful wherever analog signals must be sent from one location to another that is separated by time, space, hazards, or a noisy environment. To cope with the last three, the input signal is converted to a train of pulses, transmitted (either directly over wires, or, by modulating a carrier, via radio) to the destination, then converted back to analog (or to digital) by a f/V converter (or a counter). For compression of signals having extremely-wide dynamic ranges, log-antilog converters, such as the 755*, may be used ahead of the VFC and following the FVC.

To deal with *time* separation, V/f's make excellent modulators for multi-channel recording (and subsequent playback) of analog data, even at dc, using low-cost audio tape recorders. A VFC is used for each data channel to be recorded. The current inputs are used to bias each converter to a different zero-signal frequency, and the inputs are scaled so that there is adequate channel separation between the output frequency bands of the several VFC's. Their individual outputs are passed through flip-flops to produce symmetrical square waves of ½ the original frequency. These are then low-pass filtered and summed (with a resistor network and/or op amp) to drive the tape-recorder input.

At the recorder output, band-pass filters are used to drive f/V converters (one filter and converter per-data-channel). The FVC outputs are offset by an amount necessary to compensate for the original offset applied to each VFC input. The output of each FVC is then a replica of the (narrow-band) analog signal applied to the input of the corresponding VFC.

Other uses of V/f conversion include feedback control, phase-locked loops (VCO's), alarm-setting devices, and special-purpose digital panel meters.

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*Use the reply card to request information on high-accuracy dividers, such as the one-quadrant 434 (YZ/X) and the two-quadrant 436 (10Z/X).

*Use the reply card to request data on Analog Devices log converters, such as the 755, the 752, or the 757 log-ratio module.

MONOLITHIC 10-BIT CMOS MULTIPLYING DAC

Provides Direct Interface to Data Bus Inputs

Accepts Parallel or Serial Data, TTL or CMOS Logic

by J. Whitmore

A rapidly-expanding microprocessor market has created a need for inexpensive input/output peripherals, such as A/D and D/A converters. The ideal microprocessor analog-to-digital interface circuit would be a monolithic IC for small size and low cost, would consume little power, would interface directly to commonly-used logic levels (TTL, CMOS), and would require little, if any, external logic circuitry to communicate with the CPU data bus. A second-generation monolithic CMOS D/A converter, the AD7522, like its companion A/D converter, the AD7570*, was designed with the above requirements in mind.*

The AD7522 is a systems-compatible 10-bit multiplying D/A converter, fabricated on a single 3 x 2.2mm (118 x 89 mil) silicon die, and packaged in a 28-pin plastic or ceramic dual in-line package. Like the first-generation AD7520* multiplying D/A converter, it has 10 SPDT N-channel current-steering switches and a thin-film-on-CMOS R-2R ladder attenuator for current weighting. *In addition*, it has a dual-rank input storage system consisting of 10 "D"-type level-triggered holding latches and a 10-bit edge-triggered serial/parallel input-loading register (which in turn consists of 2 controllable "bytes", of 8- and 2-bit capacity), as shown in Figure 1.

Basic unipolar operation (either fixed-reference or 2-quadrant multiplication) requires only the addition of an external positive-or-negative, constant-or-variable, "reference" voltage or current and an operational amplifier (Figure 2). For bipolar conversion (4-quadrant multiplication), with offset-binary or 2's complement coding, one additional operational amplifier is needed.

The main (V_{DD}) supply requires a nominal +15V @ 2mA *max*; 1μA is typical, since most of the current is required only during switching. The choice of the logic (V_{CC}) supply depends on the logic-interface requirement. For example, if V_{CC} = +5V, the digital inputs are TTL-compatible. If V_{CC} = +10V to +15V, the digital inputs-and-outputs are CMOS-compatible.

Three grades of conversion linearity are offered – 8, 9, and 10 bits. Typical current-settling time following a full-scale code change on the digital inputs is 500ns.

The most-interesting aspect of the AD7522 to the system designer is the DAC's double-buffered input structure, which offers tremendous versatility, yet is seldom found even in discrete-module D/A converters. Salient features include:

1. Logic-controlled choice of serial or parallel loading.

2. A "load/display" choice, which either allows new data to update the DAC, or locks out unwanted data appearing at the digital inputs. If the AD7522 is used with a CPU data bus, this "lockout" function allows the CPU or other I/O peripheral to place data on the bus without altering data that was previously loaded into the AD7522.

3. Byte-serial (or -parallel) loading allows a 10-bit word to be loaded into the DAC from either an 8-bit micro-computer data bus, or from a 10-or-more-bit paralleled line.

4. A serial *output* allows recovery of data from the input register.

5. A short-cycle feature allows 8 bits, to the MSB, to be loaded serially.

A summary of the AD7522 functions, and where to find them in Figure 1, is given on the facing page.

The advantages of ADI's thin-film-on-CMOS process for D/A and A/D converters have been discussed in detail in earlier editions of this Journal[1,2]; briefly summarized here, they are:

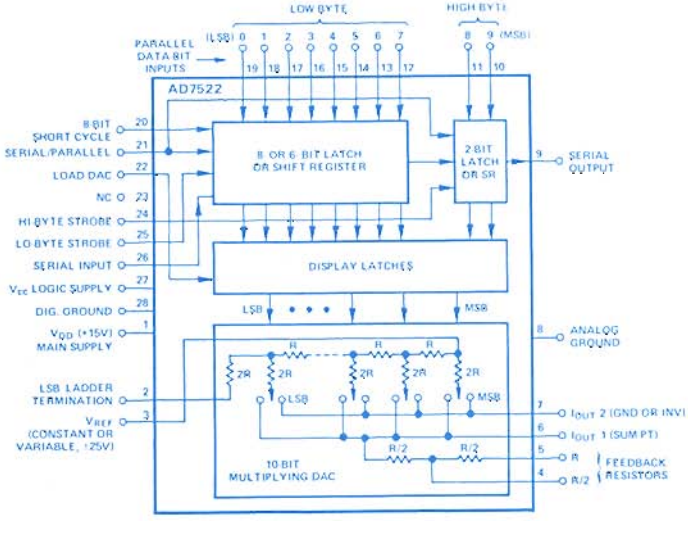

Figure 1. Functional diagram of the AD7522

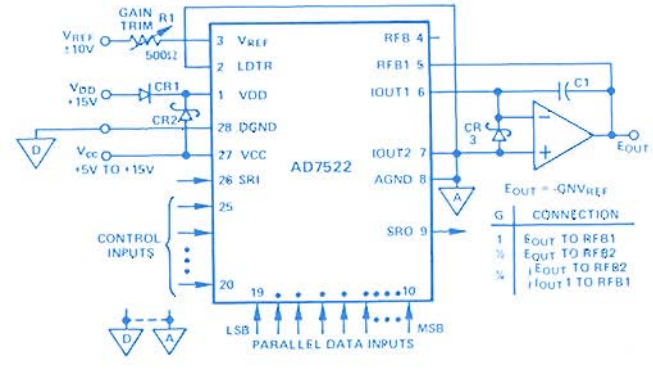

Figure 2. Connecting the AD7522 for unipolar D/A conversion. N is a fractional 10-bit binary number from 0 to $(1 - 2^{-10})$.

*Use the reply card to request technical data on any of these products.

[1] "A 10-Bit Monolithic CMOS D/A Converter", *Analog Dialogue*, Number 8-1 (1974).

[2] "10-Bit Monolithic CMOS Analog-to-Digital Converter", *Analog Dialogue*, 9-2 (1975).

- High logic density and low dissipation (hence good yields and low cost).
- No β and V_{BE} problems.
- Since switches are bidirectional, both polarities of analog signals are inherent.
- SiCr resistor networks have better linearity and tracking than diffused resistors.

APPLICATIONS

The AD7522 can perform all of the conversion functions that are performed by the AD7520, but with the added flexibility of communication with digital systems. However, as a second-generation DAC, it has a few improvements that facilitate analog applications as well. First of all, there are separate analog and digital ground returns. Figure 2 shows how the AD7522 is connected for a unipolar conversion relationship. The feedback resistor is center-tapped, which allows a choice of full-scale gain of 1, ½, or ¼. The termination of the ladder, instead of being grounded internally, is brought out to a terminal; this permits bipolar (4-quadrant multiplier) circuits to be instrumented with fewer external resistors than is the case with AD7520.

Two, among many, of the digital-communication possibilities are shown in Figures 3 and 4. Figure 3 shows how the AD7522

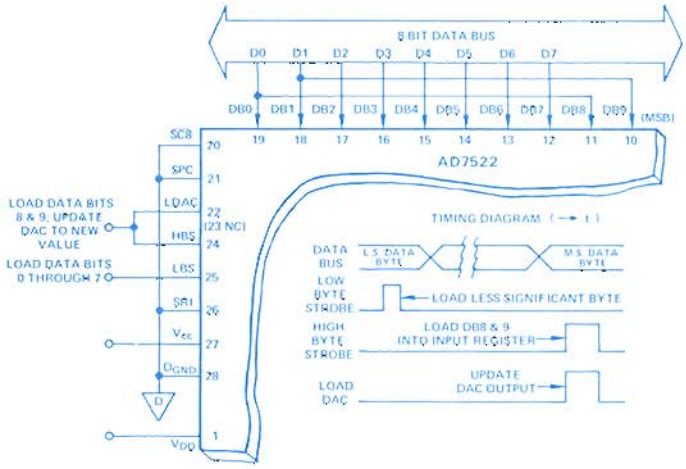

Figure 3. Loading a 10-bit word from an 8-bit data bus in 2 bytes. For clarity, analog connections are omitted.

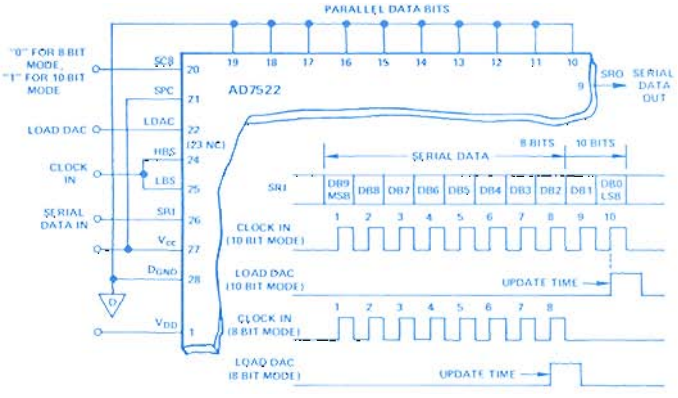

Figure 4. Serial 8- and 10-bit loading. Analog connections omitted.

might be connected to an 8-bit microprocessor bus, for byte-serial updating. In this example, it is hard-wired into the parallel mode; bits 0 through 7 are connected to D0 through D7 of the bus; bits 8 and 9 (MSB) are connected to D0 and D1. "Low Byte ENable" loads bits 0 through 7; "High Byte ENable" loads bits 8 & 9; then Load/Display DAC Strobe loads the DAC when desired. Figure 4 illustrates serial operation.

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AD7522 FUNCTIONS AND THEIR CONNECTIONS

(Refer to Figure 1)

FUNCTION	PIN NO.	MNEMONIC NOTATION
DIGITAL – Data (positive-true with respect to $I_{OUT}1$)		
Parallel Data Input, Data-Bit 9 (MSB) to Data-Bit 0 (LSB)	10–19	DB9 through DB0
SeRial Input	26	SRI
SeRial Output (NRZ) – Auxiliary output for recovering data stored in the input register	9	SRO
DIGITAL – Control		
Serial/Parallel Control – If "0", parallel data will be loaded into input registers DB0–DB9 when LBS and HBS are exercised; if "1", serial data will be shifted through input registers when clocked in with LBS and HBS.	21	SPC
High-Byte Strobe – In the *parallel* mode, positive edge strobes parallel data appearing on DB8 and DB9 into the input register; in *serial*, positive edges advance data through the input shift register.	24	HBS
Low-Byte Strobe – Same functions as HBS, for DB0 through DB7	25	LBS
Load/Display DAC Strobe – If "0", AD7522 is in "display" mode, digital activity in input register is locked out; if "1", data in the input register is strobed into the DAC.	22	LDAC
Short-Cycle (8 bits) – In *serial*, if "0", 2 LSB's are bypassed for proper loading of 8 bits; if "1", a full 10-bit serial word is accepted.	20	$\overline{SC8}$
ANALOG		
Reference Input – Constant or variable ac or dc voltage in the ±25V range is proportionally scaled (gain-adjusted) by the input digital word.	3	V_{REF}
Output Current – Normally connected to summing point of the output op amp; bit-currents flow for "1" DB's.	6	IOUT1
Complementary Output – Normally grounded (unipolar) or connected to summing point of inverting op amp (bipolar); bit currents flow for "0" DB's.	7	IOUT2
Feedback Resistor (F.S. Gain = 1) – One end is connected internally to $I_{OUT}1$. RFB1 is connected to op-amp output for normal unity-gain operation, or to summing point for gain of ¼; no connection for gain of ½.	5	RFB1
Feedback Resistor Center-Tap (F.S. Gain = ½) – Connected to op-amp output for gain of ½ or ¼.	4	RFB2
Ladder Termination – Grounded for unipolar gain; connected to $I_{OUT}2$ for bipolar gain.	2	LDTR
SERVICE		
Main Supply – +15V nominal	1	VDD
Logic Supply – +5V for TTL compatibility; +10V to +15V for CMOS compatibility	27	VCC
Digital Ground	28	DGND
Analog Ground – Back gate of the DAC's N-channel single-pole, double-throw (SPDT) current-steering switches.	8	AGND

GET THE MOST FROM PRECISION R-NETWORKS

Avoid These Common Pitfalls in Resistance-Network Design

by Lavar Clegg

Precision resistor-networks are enjoying rapidly-increasing popularity because of their convenience, increased availability*, and decreasing cost. Not only are they replacing matched discrete-resistor assemblies, but they are also finding uses in applications where precision resistors had previously been avoided. Among the important advantages of thin-film monolithic networks are high accuracy, close resistor-matching and -tracking, low temperature-coefficient-of-resistance (TCR) and wide range of resistance values. As one might expect, their many advantages are accompanied by some design hazards. Here are a few kinds of trouble that you should seek to avoid in your application, whether you're using a standard part or initiating a custom design. Treat your network with respect and understanding; it will pay you back by behaving predictably.

1. LEAKAGE CURRENTS

Figure 1 shows a decade attenuator designed to attenuate a 100V input down to 10V, 1V, 0.1V, and 0.01V with 0.1% accuracy, while maintaining an input impedance of 1MΩ and equal output impedances of 100kΩ (unused outputs open-circuited). Here is how leakage can undermine the accuracy of this network:

First, it is manifest that leakage paths across high-value resistors should be avoided. Here, the effective shunt resistance in path R1 (internal and external strays) should be greater than $10^9\Omega$, to avoid leakage errors greater than 0.1%; this situation is easy to see and to deal with.

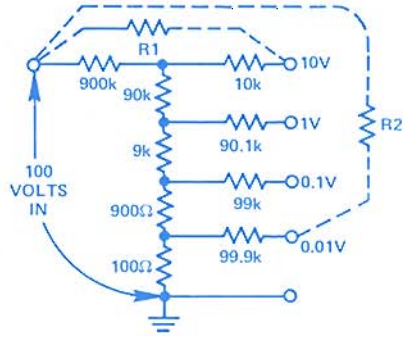

Figure 1. Decade attenuator

More recondite is path R2, a leakage path from the input to the lowest-level output. A voltage error of 10μV (0.1% of 10mV) could be contributed by the voltage drop of a leakage current of $(10^{-5}\,V)/(10^5\,\Omega) = 10^{-10}$ A in the 99.9kΩ output resistance. A current of this magnitude would require a leakage path, from the 100V input, of $(100V)/(10^{-10}A) = 10^{12}\Omega$! Such leakages occur readily and their presence can be easily overlooked. They can be caused by minor contamination on boards and leads, and inadequate separation of conductors. The outputs should be well-separated from the inputs (guarded if possible), both in the external circuitry and in the basic design of the network. Cleanliness is of course mandatory.

*Use the reply card to request ADI's 16-page *Resistor Book*.

2. TERMINAL RESISTANCE

It is manifest that "conductors" are also resistors. Their resistance must be considered when dealing with precision-resistor networks that include low resistance-values. Series resistance of conductors is particularly significant in networks that include both high- and low-resistance values, such as in the network of Figure 1. In addition to the effect on *total* resistance, there can also be an increase of the *overall* TCR; since conductors have a very high TCR, it takes only a few milliohms of metallic resistance in series with a 100Ω resistor to degrade the overall TCR. The designer must consider series resistance, both in the network and in the environment, including internal-metallization connections, network leads, solder joints, and circuit-board connectors.

Figure 2 shows an example in which an additional 3.5ppm is added to the TCR of the resistance in question. In a network, it would impose a 3.5ppm/°C *tracking error* with respect to the higher-value resistances, using the reasonable assumption that inherent tracking of the resistance elements alone is considerably better.

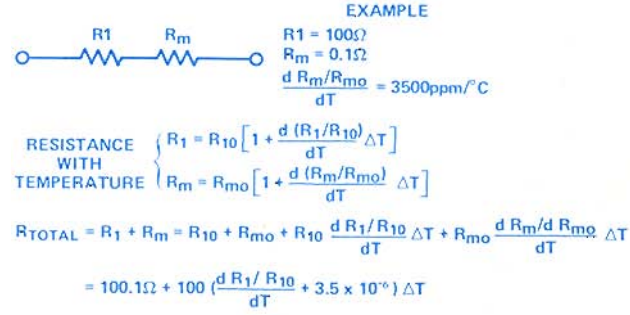

Figure 2. Effect of small series resistance with high TCR

3. WHERE IS THE NODE?

When resistors in a network have a common terminal, a question may arise as to whether the intended circuit-node is at the internal connection point or at the terminus of the connecting lead. If current is to flow externally, there will be a voltage drop across the resistance in series with the connecting lead. The simple network in Figure 3 illustrates the principle. In the ideal circuit (a), pin 2 and point Y are identical. In the actual circuit, the values of R_1 and R_2 appear in series with the resistances R_m, and the lead to the node also has resistance, R_m. In designing the overall circuit, one must consider not

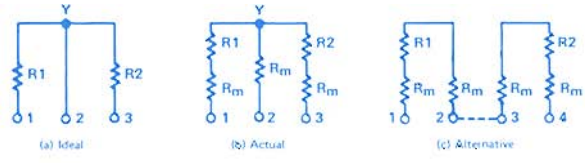

Figure 3. Node ambiguity

only the lead resistance in series with the resistors, but also – if current flows through pin 2 – the drop across the common resistance R_m. If the voltage actually appearing at the node

must be accurately determined, the configuration of (c) may be more desirable, despite the fact that the individual resistances become $R_1 + 2R_m$ and $R_2 + 2R_m$. On the other hand, the configuration of (c) is less desirable than that of (b) if the lead to pin 2 carries no current.

The user should therefore be careful to determine the actual location of the nodes when the circuit is used in his system and to analyze the effects of current flow. As a rule, this problem arises when R values are 1kΩ or less and required accuracies are 0.05% or better.

4. POWER TRACKING

A network may be well-characterized by a tracking TCR specification, accuracy over the specified temperature range, and a voltage coefficient of resistance (essentially negligible for ADI's thin-film networks), yet the tracking accuracy may deteriorate when the input voltage is changed, if the network has been improperly specified for dissipation. Here's why:

Each resistor dissipates energy, depending on the applied current or voltage. Because the substrate is not a perfect heat sink, there will be a small local temperature rise, which will cause an increase in resistance, via the absolute TCR of the device. (Although the absolute TCR should ideally be zero, it is more likely to be about 25–50ppm/°C for practical high-precision devices.) Even though the resistances will track nearly perfectly for ambient temperature changes, the changes in resistance caused by local heating depend on the power density of the energy dissipated in a given resistor.

If the voltage applied to the resistor changes, there will be a change in dissipation, hence temperature, hence resistance. Unless the change in dissipation associated with the applied voltage change causes all the interconnected resistors to experience the same temperature change, their resistances will change at different rates, causing increased errors. For example, if the network of Figure 1 were properly designed, with uniform current density in all of the decade resistors, so that the self-heating per-unit-resistance is the same for all of the resistors, the designated ratio-accuracy to within 0.1% could be maintained, even if the applied voltage were increased to 200V.

In this case, the network would have been designed for power tracking, i.e., each smaller resistor in the string would have 1/10 the dissipation capability of the resistor above it. If, on the other hand, all the resistors, including the low values, had been instead specified for equal dissipation capability, such an arbitrary spec, besides being unnecessarily conservative, would have compromised the accuracy spec over a range of input voltage. The moral: Make certain your network is designed for power tracking, where appropriate, rather than absolute power dissipation per resistor.

5. HOTHEADED NEIGHBOR

The heating produced by a nearby independent resistor in the same device can produce an error. Assume, for example, that in Figure 4, R1 and R2 form a precise voltage divider. R3, part of an independent circuit, has a large, varying current in it. The power dissipated by R3 varies; temperatures in its vicinity also vary. If R3 is nearer to R2 than to R1, and the resistors have a non-zero TCR, the dissipation in R3 affects the accuracy of the R1-R2 voltage divider.

Thermal coupling and its effects can usually be minimized by network design – proper resistor size, location, and orientation. Though often a minor source of error, it is worth considering when planning circuits with accuracies to within 0.05% or better. Pay particular attention to it when resistors are subject to widely-varying voltages.

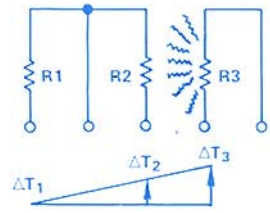

Figure 4. Thermal gradients

6. CAPACITANCE

All resistor networks exhibit some capacitance. It must be considered whenever fast settling time is required or a wide frequency range is needed. The equivalent circuit of a resistor can be quite complex if one seeks to consider *all* reactance effects. The dominant capacitive reactances in networks are lumped capacitance between resistors and distributed capacitance within a resistor. The shunting effect of the latter is aggravated by high resistance values.

Generally, low-value resistors should be used when speed and frequency range are important. Although the terms are relative, "low" might imply values around 5kΩ, and "high" 100kΩ. Despite the capacitance, networks can be designed for optimum response, by the matching of time-constants.

The most-important consideration is the substrate material. Glass or ceramic will provide the least capacitance. Oxidized silicon will provide the most capacitance, because it is conductive under the oxide layer. Silicon substrates are usually avoided for high-speed networks, but careful design and processing can still provide circuits with excellent dynamic performance – as in the case of the AD562 D/A converter.

Next, one must consider the distributed capacitance. It cannot be eliminated, but response can be optimized by designing the resistors for equal distributed capacitance per unit of resistance. This may have to be done at the expense of other parameters, however, such as power-tracking, dissipation, or pin-out. Matching the distributed capacitance of resistors comprising a wide range of resistance is difficult. For example, the network of Figure 1 could be optimized in terms of response for a group of about 3 resistors in the decade string. To optimize all 5 would be very difficult.

When speed is important: use as low a resistance as possible; use a network construction that minimizes capacitance; and specify or select a network which is designed for equal distributed-RC-time-constants.

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At the time this was written, Lavar Clegg was Manager of Engineering at our Resistor Products Division. His photo and a brief biographical note appeared in *Analog Dialogue* 8-1. He is no longer at ADI.

DPM's: THE SECOND GENERATION

LSI and Big LED's Promise:

Easier Reading, Lower Cost, Improved Reliability

by Jim Hayes

Even as we introduced the models that completed the "First Generation" of Analog Devices panel meters, the second generation was in the final stages of engineering. The first generation, as users know, consisted of both +5V logic-powered units and ac line-powered devices, using TTL small-scale integrated circuits for logic, linear IC's and discrete components for analog circuitry, and a "mixed bag" of displays.

The availability of MOS-LSI (metal-oxide semiconductor – large-scale integration) integrated circuits promised that newer designs would have greatly-reduced component count and lower power consumption, both of which would foster better reliability and lower cost. Another technological development with great promise was the availability of improved LED's (light-emitting displays) with larger digit-size, greater intensity, and significantly lower cost.

The massive engineering program set up to evaluate the possible DPM applications of these new technologies has led to a completely-new line of digital panel meters. The first three members of this "new generation" are described here. They are:

- AD2021 3½-Digit Logic-Powered DPM*
- AD2024 4½-Digit Line-Powered DPM*
- AD2027 4½-Digit Logic-Powered DPM*

BENEFITS OF "2nd-GENERATION" DESIGNS

The term "second generation" implies something more than cosmetic changes. Through the use of the newer technology – and experience gained with their predecessors, the new DPMs offer a number of advantages. The AD2021, for example, has a parts list 42% shorter than that of its first-generation counterpart, the AD2010, and it uses two circuit boards instead of three. The smaller number of components and p.c. boards means fewer mechanical interconnections and promises increased reliability. The MOS-LSI circuitry of the AD2021 uses 42% less power than that of the AD2010, which results in a correspondingly lower temperature rise, again contributing to greater reliability. You'd also expect a corresponding decrease in the power supply requirement (hence power supply cost), and, in fact, the power requirement at +5V is reduced to 300mA. The AD2027 also shows a similar decrease in power consumption over the AD2004, its progenitor.

The ac-powered AD2024, although similarly improved, naturally has to cope with the inefficiency inherent in power supplies, an inefficiency of power, space, and cost that dilutes the effect of improvements to the basic meter circuitry. On the other hand, though, for applications that require ac power, the reduced space and power requirements of the basic meter circuit, as well as its increased reliability, become of great importance.

LOGIC POWER IS THE LOGICAL CHOICE

The MOS-LSI circuitry used in these new DPMs was only a laboratory curiosity at the time that Analog Devices introduced the first +5V logic-powered DPM. But instrument- and system-designers recognized the possible cost savings from powering the DPM from the same supplies as their other circuits, as well as the possibility of putting the much-smaller logic-powered DPM into systems that had little space for a bulky line-powered unit. The 5-volt units gained immediate acceptance and are now in widespread use.

Today's forward-looking instrument-designer concentrates on taking advantage of the same LSI concept that has made these 2nd-generation DPMs possible, in quest of smaller, lighter instruments, often with portability in mind. Thus, DPMs like the AD2021, which uses a total of only 1½ watts, become a logical choice for incorporation in such instruments.

Microprocessors are another popular component starting to appear with increasing frequency in new instruments. These new DPMs will not only be able to use readily-available logic power, but in addition, their data outputs are in a bit-parallel,

AUTOMATIC TESTING

The Universal Tester is a key tool in reducing the cost of second-generation devices and insuring faster, more-thorough testing of DPM parameters. It typically performs 36 tests involving 14 parameters, individually tailored to the specific device type by automatic programs using RAMs and ROMs.

With halts only for trim adjustments, it performs a complete set of tests in about 35 seconds, resulting in substantial cost savings, yet more-comprehensive testing than in the past.

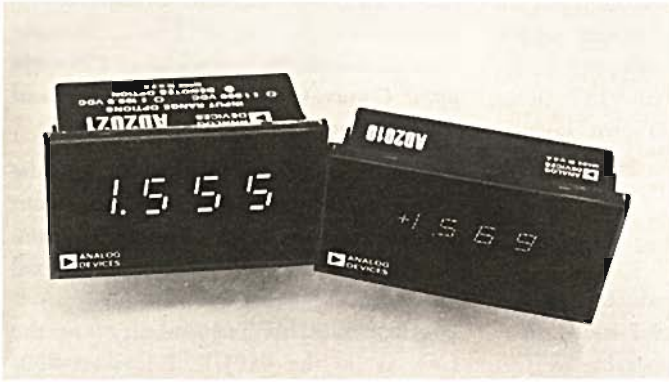
Here, AD2021s are being tested after the completion of 168-hour burn-in. When the test is completed, they will undergo a final Q.C. inspection before shipment.

*Use the reply card to request data on these products.

character-serial format, which makes interfacing with microprocessors easier to implement than did the full parallel format of the earlier designs. The data outputs are, of course, compatible with the MOS logic systems used by the majority of microprocessors.

LARGER, BETTER-LOOKING DISPLAYS

The second-generation DPMs use large LED displays of the "light-pipe" design. These displays show large bar segments, rather than a line of dots, which makes them more pleasing to the eye than were the earlier LED designs. They are almost twice the size of the LEDs used earlier: 13mm (0.5") on the AD2021 and 11mm (0.43") on the AD2024 and AD2027, as compared with 7mm (0.27") on the earlier AD2004 and AD2010. The new display characters are almost as large as those in the Beckman gas-discharge display. The new displays therefore offer the visual appeal of a large shaped-character display combined with the reliability of a low-voltage solid-state device.



The AD2021 has displays that are 85% bigger than those of the first-generation AD2010.

ARE THEY BETTER IN EVERY WAY?

That depends on your point of view. We mentioned the fewer parts and lower power consumption, but the bit-parallel, character-serial data outputs may be a mixed blessing for some users. Although the output format may be ideal for interfacing to microprocessors (and "eyes only"), such devices as digital printers and comparators generally require conversion to parallel format. For convenience, this conversion will be available as an extra-cost option on the AD2024 and the AD2027, using an extra circuit board and card-edge connector. The small case size of the AD2021 prohibits *internal* incorporation of this option, but the data sheet shows the rather simple connection scheme required for latching the data in a parallel format externally.

Except for this consideration, virtually all performance features are comparable to those of the first-generation DPMs. Accuracy, stability, and general performance characteristics meet the same high standards our users have come to expect from Analog Devices DPMs. Only the new 4½-digit models show any compromise: they use a limited differential input rather than the opto-isolated floating input of earlier designs.

ALL THIS AT LOWER COST?

An important advantage of these second-generation designs is their lower cost. The combined advantages of the lower component count and cost, as well as the reduced cost of manufacturing, make these DPMs up to 37% lower in cost than their predecessors, with the greatest improvement in the 4½-digit units.

THE PRODUCTS THEMSELVES

The AD2021 is available with full-scale ranges of ±199.9mV or ±1.999V full-scale. Provision is made for attenuators for special input ranges.

- *AD2021*: 3½-digit, logic-powered (+5VDC). Measures voltage over full-scale range of ±1.999VDC (S option: ±199.9mVDC) with an accuracy of ±0.05% of reading ±0.025%FS ±1 digit. "Limited differential input" prevents ground loops and provides 35 to 50dB of CMR at common-mode voltages up to ±200mV. Normal-mode rejection is 40dB at 50–60Hz. BCD outputs in bit-parallel, character-serial format compatible with CMOS logic systems. Controls to hold readings, select decimal points, and blank the display are provided. Packaged in ADI's logic-powered-DPM case, only 32mm (1.25") deep; panel cutout, now used by several other manufacturers, allows mechanical second-sourcing. The AD2021 uses same pin connections as the AD2010 (except for BCD outputs), for convenience of users in updating designs. $128 (1–9).

- *AD2024 and AD2027*: 4½-digit, logic-powered (AD2027) or ac-line-powered (AD2024). Measure dc input voltages over full-scale range of ±1.9999V, with accuracy of ±0.005% of reading ±0.005% of full scale ±1 digit. CMR is 50dB with common-mode voltages to ±200mV; normal-mode rejection is 25dB @ 50–60Hz. BCD outputs in bit-parallel, character-serial format; parallel TTL-compatible outputs optional. Both types are housed in cases of size compatible with U.S. industry standards for ac-line-powered and logic-powered types, respectively. AD2024: $207 (1–9), AD2027: $197 (1–9).

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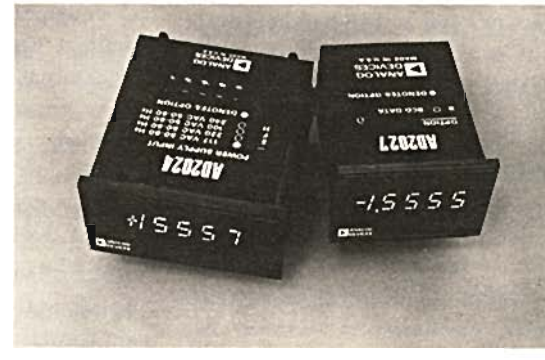
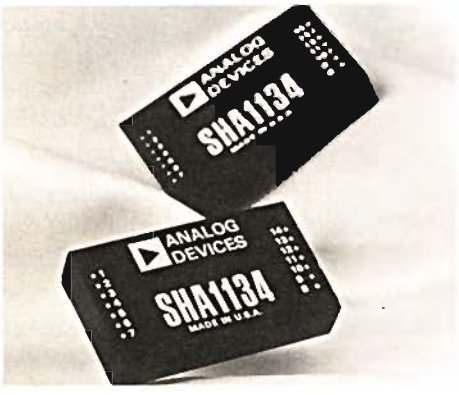


The AD2024 and AD2027 have identical features and specifications, but each is packaged in the appropriate (U.S.) industry-standard cases for line-powered or logic-powered units.

SAMPLE-HOLD
For "12-Bit" Data
Low Cost ($75-100's)



Model SHA1134* is a low-cost sample-hold amplifier with an acquisition time of 3.4μs, packaged in a compact 29 x 51 x 10mm (1 1/8" x 2" x 0.4") module. It is half the size of and 30 percent faster than its predecessor, the SHA-1A, yet costs only 2/3 as much. Available from stock; price is $75 (100's), $99 (1–9).

Its ±0.005% maximum linearity error and 50μV/ms droop rate make it suitable for use with virtually all 12-bit successive-approximation A/D converters. Indeed, its 3.4μs acquisition time, 35ns aperture delay, and 2ns aperture jitter make the SHA1134 compatible with all but the very fastest 12-bit converters.

When in the *sample* mode, it appears as a fast amplifier with a 3.2μs settling time to accuracy within 0.01%. When switched to the *hold* mode, its output settles to the final value within 1μs.

The SHA1134 also has a $10^7\Omega$ minimum input resistance and a -3dB bandwidth (in *sample*) of 800kHz. The operating temperature range is 0° to +70°C. The SHA1134 operates from the usual ±15V supply; no adjustment pots are required. The operating modes are controlled by a DTL/TTL-compatible logic input.

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*For technical data on the SHA1134, use the reply card.

V/f CONVERTER FAMILY
Economy, Accuracy, and Versatility in
Six New 10/20kHz (Full-Scale) Modules

Having been introduced to V/f's (pp. 6–9), the reader whose appetite has been whetted can consider this variety of newly-introduced modules, now in stock (and the promise of more to come):

- Model 450J/K* for High Performance
- Model 456J/K* for Economy
- Model 454J/K* for Versatility

The 1kHz/V model 450K, the highest-performer in this group, has nonlinearity of ±50ppm *max*, stability to within ±25ppm/°C *max*, and an effective 13-bit accuracy over the 1mV to +15V signal range. The 450J provides cost savings, with almost-comparable performance, ±100ppm *max*, and ±50ppm/°C *max*. Prices of both are reasonable: J, $49, K, $59 (1–9).

The 1kHz/V model 456J, the lowest-cost member of the family, and its brother, the 456K, maintain respectable performance: linearity within ±0.03% (0.02%)

max and stability to within ±120 (80) ppm/°C *max*. Cost is $34 ($42), 1–9, and the J is a low $25 in 100's.

The most versatile of the devices, the 454J/K have both voltage and current inputs, with transfer functions of 1kHz/V and 30kHz/mA, respectively, and normal full-scale ranges of +20V and (2/3)mA → 20kHz. Linearity and stability are the same as for the 450J/K. Prices are $53/$62 (1–9).

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HIGH-SPEED 12-BIT DAC
DAC1108 Has 15ns Settling to<0.01%

The DAC1108* is a 12-bit digital-to-current converter that combines fast 150ns settling to within 0.01% with compact 51 x 51 x 10mm (2" x 2" x 0.4") package size.

It includes a precision temperature-compensated reference source, high-speed current-steering switches, and a carefully-trimmed network of weighting resistors. No external adjustments are needed; only ±15V power is needed for operation. Although the DAC1108 features 12-bit linearity, its low price is competitive with those of many 10-bit DACs; the settling time of the DAC1108 to within 0.05% is a fast 60 nanoseconds.

The digital inputs are fully DTL/TTL-compatible. For unipolar applications, they accept binary coding; for bipolar applications, the code is offset binary. If the most-significant bit is complemented, 2's complement coding may be used.

The +5mA or ±2.5mA current output may be applied directly to an external resistor to develop a voltage output, or it can be applied to the input of a fast-settling op amp, such as the modular model 50* or the integrated-circuit AD509K* for amplification or impedance transformation.

The fast settling of the DAC1108 makes it ideal for such high-speed applications as computer-driven displays, automatic test equipment, and function generators. The DAC1108 operates over the 0° to +70°C range. Delivery is from stock. Price is $122 (1–9), $104 (100's).

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*Use the reply card to request technical data on these devices.

TRUE-RMS to DC CONVERTER

High Accuracy at Low Cost Without Trimming

Works Well With Crest Factors up to 10

Model 441* is a very-low-cost, true-RMS to dc converter offering performance comparable to that of higher-priced units. The log-antilog circuit design of the 441 enables the user to perform high-accuracy measurements (0.2%, 441K) on simple ac signals, such as sine waves, and on a wide range of complex waveforms (accuracy to within 1% for crest factors up to 10). In addition, the model 441 can directly measure the rms value of a waveform containing both ac and dc components. Figure 1 is a plot of reading-error as a function of crest factor.

Unlike some types of low-cost rms devices, which require complicated, iterative, and otherwise time-consuming trim procedures in order to deliver acceptable performance (and then only for sine waves), the model 441 needs no external adjustments to achieve its specified performance.

With the use of simple, optional, external trims, for scale factor and offset, initial accuracy can be further improved. Provisions are also made for the addition of an external capacitor to achieve errors approaching 0.1% at frequencies below 100Hz without affecting the bandwidth for higher-frequency inputs.

The model 441 is capable of operating over a wide range of power-supply voltages (±4V to ±18VDC at 10mA), making it a near-ideal choice for use in portable, battery-operated designs. Performance specifications at low supply-levels are the same as at higher supply voltages, except that maximum output signal and input signal range decrease directly with power-supply voltage. The 441 can typically accommodate a peak input signal-level of up to (V_S -3) volts, which enables it to handle a 1-volt peak input when V_S is at the minimum specified value of 4V.

Crest factor is frequently understated in importance for rms measurements, yet it is the key to determining the accuracy of true-rms measurements on a specific waveform. Crest factor is the ratio of (the larger of positive or negative) peak input to the rms value of the signal. Tables of crest factor as a function of waveform are given on data sheets of Analog Devices rms products, and, more completely, in the *Nonlinear Circuits Handbook*†.

Model 441 maintains rated measurement accuracy for signals with crest factors up to 3, and provides 1% maximum error for signals with crest factors up to 10, as shown in Figure 1.

The 441 is available in two accuracy-grades (441J and 441K), packaged in a 51 x 51 x 10.4mm (2" x 2" x 0.4") module. Price is $45/$55; the "J" version costs as little as $28 in 100's.

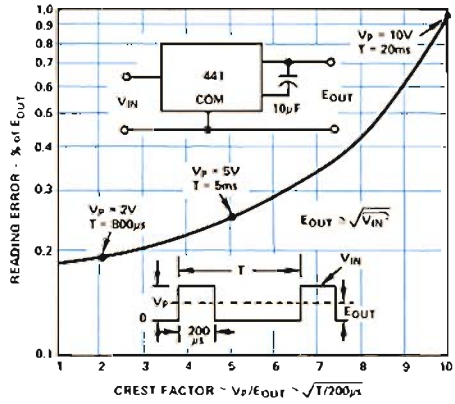

Figure 1. Reading error vs. crest factor (constant RMS = 1V) for model 441.

The excellent performance and economy of the 441J, plus its pretrimming and wide power-supply repertoire, make it ideal for a wide range of rms-measurement applications, both in the laboratory and in the field. Typical applications include sound and noise-level instrumentation; vibration analysis; SCR controller and power-line measurements; telephone, telegraph, and modem test-equipment; and all sorts of rms instrumentation functions in instruments, apparatus, and systems.

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*Use the reply card to request information on the 441.

†Published in 1974, available from ADI @ $5.95.

I.C. OP AMP

Laser-Trimmed

V_{OS}<100μV, $5.95(100's)

The AD510* is a high-precision op amp having low offset and drift, internal compensation, and protected inputs.

Performance features such as 25μV maximum offset and 0.5μV/°C drift (AD510L) are made possible by the combination of laser-trimming at the wafer stage (see page 3) and a patented thermally-balanced chip layout. The internal compensation eliminates the need for external capacitors that characterizes some low-drift amplifier types, such as the 725.

In keeping with the requirements of a precision op amp, the AD510 also offers bias and offset currents as low as 10nA max and 2.5nA max, respectively (AD510L). Input noise is a low 1μV p-p in a 0.01 to 10Hz bandwidth. Open-loop gain is maintained at over 10^6, even under loaded conditions. The thermally-balanced chip layout makes the AD510 practically immune to temperature gradients across the monolithic chip caused by current loads at the output. The AD510 is designed for applications requiring high accuracy at the lowest possible cost, such as bridge instrumentation, stable references, followers, and analog computation. Being pin-compatible with 741-type amplifiers, the AD510 should also be considered for economical upgrading of existing 741-based designs.

Bootstrapping of the critical input transistors produces 110dB minimum CMR. The fully-protected inputs tolerate differential input voltages of up to ±V_S without gain or bias-current degradation caused by reverse breakdown. The output is short-circuit protected and drives 1000pF of load capacitance without oscillation.

The AD510 is packaged in a hermetically-sealed TO-99 can. It is available in three versions (J, K, L) for 0° to +70°C operation, and one (S) for operation over the full -55°C to +125°C "military" range. All versions are available from stock.

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*Use the reply card to request a data sheet on the AD510.

EASY-TO-USE SERDEX SUBSYSTEMS

They Interface Parallel Digital Data with Asynchronous Serial ASCII-Compatible Teletypewriters or Computers

Since Analog Devices first introduced SERDEX (SERial Data-EXchange) Modules* in these pages (Volume 7, No. 2), our users have designed them into a wide variety of data-logging and process-control applications. SERDEX now provides a convenient interfacing medium for data communication in research laboratories (between analytical instruments and teletypewriters and computers) and in a variety of environmental-monitoring systems.

SERDEX users comment that they like the simplicity of the hardware interface that SERDEX provides and the ease of writing computer software, since SERDEX systems are programmed in high-level languages, such as BASIC, exactly the same way one programs data-inputting and outputting with teletypewriters.

But, as with any innovative approach, life is not entirely a bed of roses. Users who designed SERDEX into systems that are built in production quantities simply used them as another component on their system cards, were able to realize the resulting economy, and never had much head-scratching about the interconnections.

On the other hand, users who employ SERDEX in one-of-a-kind systems have commented about the complexity of wiring interconnections between the modules, a condition caused in part by the extreme flexibility and conceptual elegance of the design.

As an aid to designers who prefer simplicity to flexibility, we've now designed a series of SERDEX Subsystems that perform the complete Transmitter, Receiver, and Multiplexer functions. Each "Subsystem"* is on a 114 x 203mm (4½" x 8") circuit board that fits into a standard 4½" card cage and requires +5V only for operation.

TELL ME AGAIN – WHAT'S SERDEX?

SERDEX, for SERial Data EXchange, is a series of modules which convert parallel digital data into asynchronous serial ASCII data (American Standard Code for Information Interchange), convert ASCII into parallel data, and multiplex any number of either function into large systems. The parallel data is associated with standard system components, such as A/D converters, DACs, DPMs, remote displays, and buffers. ASCII data is used as a standard 2-wire communication medium by teletypewriters, CRT terminals, and computers.

*For technical data on SERDEX modules and/or cards, use the reply card.

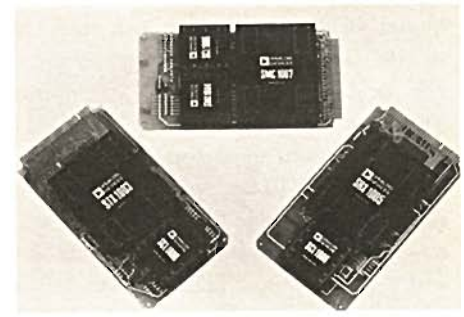
TRANSMITTER CARD

The SERDEX transmitter card, STX2603, upon command, converts parallel digital data into asynchronous serial ASCII for transmission back to a teletypewriter (or TTY port on a computer) via opto-isolated 20mA current loops or direct TTL pulses; it also has a set of control outputs, which can be used to initiate data conversion upon command or to program indicators or relays.

The STX2603 contains an STX1003 Transmitter Module, an SCL1006 Clock Module, 2 additional shift registers, and all the necessary interconnections and pullup resistors. The shift registers allow expansion of the ASCII code-transmission capability of SERDEX, for sending not only numerical data, but also symbols, such as +, -, (,), etc., and control characters, such as Line Feed and Carriage Return. For simple data-transmission applications, such as inputting data from an A/D converter or a DPM to a teletypewriter, the STX2603 requires only +5V power, a current-loop driver, and the input data to be transmitted.

RECEIVER CARD

The SERDEX Receiver Card, STX2605, converts asynchronous serial ASCII data into parallel digital data. It consists of an SRX1005 Receiver Module, an SCL1006 Clock Module, and all appropriate subsystem interconnections on a circuit board. Like the Transmitter, the SRX2605 is also easy to wire up and is ideal for programming remote digital-input devices, such as DACs and remote displays.



MULTIPLEXER CARD

The SERDEX Multiplexer Card, SMX2607 is designed to allow interfacing up to 8 STX2603 or SRX2605 cards, in any combination, to a control device via a single current loop. The multiplexer card contains an SMX1004 SERDEX Multiplexer, and SMC1007 Multiplexer-Controller, and an SCL1006 Clock. By the cascading of multiplexers, SERDEX systems can be built to economically handle thousands of channels, by techniques shown in the SERDEX-Multiplexer *Users' Guide*.

VERSATILE PROGRAMMING

The flexibility of the SERDEX *modules* is not lost to *card* users. Although cards are delivered pre-wired for communication to and from teletypewriters, at distances up to 3000m (10^4 ft), via an opto-isolated 20mA current loop at 110 baud, programming jumpers are provided to retain inherent SERDEX flexibility. With jumpers, one can program baud rate, word length, number of *stop* bits, and parity verification. Other jumpers provide for direct-coupled TTL, rather than isolated current loop, and choice of full- or half-duplex operation.

SOFTWARE AND HARDWARE

Since the cards use the standard SERDEX modules in essentially the recommended configurations, the rather-extensive SERDEX module literature is available to card users. Each card comes complete with the appropriate Users' Guide(s), instructions, and card edge-connector.

TRUE TIME AVERAGE OVER VARYING PERIODS

Versatile Time-Independent Averaging Circuit Uses IC DAC

by C. Barker

The circuit described here[1] obtains the true time average of a varying input signal over a wide range of differing periods. It was designed for use in a system for the control of plastic film-thickness, but the technique has many other potential uses. A few that come to mind include: measurements of average pressure- or volume-per-stroke in pumps and bellows, measurements of true-rms over varying periods, measurement of quasi-electrometer currents without high-value resistors, and normalized integration of one-shot phenomena.

The simple, yet effective, circuit shown here uses a standard integrating circuit and an AD7521* monolithic multiplying D/A converter in the feedback path of an operational amplifier to obtain a gain inversely-proportional to time, as determined by the count of a stream of pulses from a clock circuit (Fig. 1).

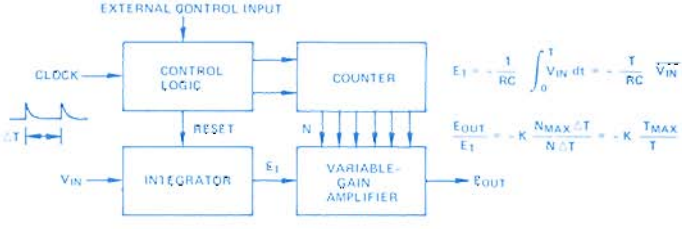


Figure 1. Block diagram of the averager. $T_{max} = N_{max}\Delta T$ is the time required for the counter to reach full-scale.

The integrator output over a time interval, T, is inherently equal to the product of the average value of the input and the ratio of T to the characteristic time, RC. The gain of the variable-gain amplifier is inversely proportional to the number of pulses, and hence to the elapsed time $N\Delta T$ (which is equal to T at each instant the count is updated). The output is

$$E_O = \left[\frac{T}{RC}\,\overline{V_{IN}}\right]\left[\frac{KT_{max}}{T}\right] = \left[K\,\frac{T_{max}}{RC}\right]\overline{V_{IN}} \qquad (1)$$

E_O depends only on $\overline{V_{IN}}$ and is essentially independent of T.

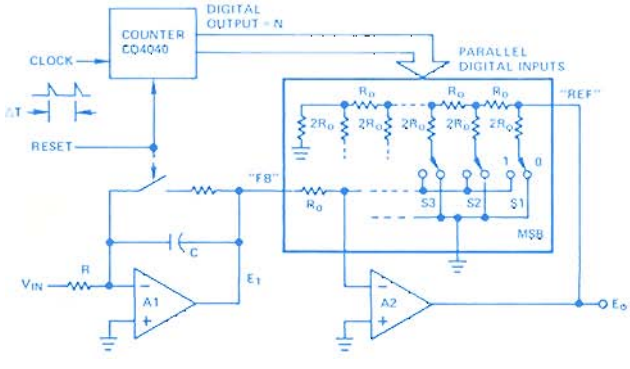


Figure 2. Simplified circuit diagram

The variable-gain amplifier (Figure 2) consists of a D/A converter in the feedback path of an operational amplifier. The converter used here is the 12-bit AD7521, which consists of an R-2R ladder attenuator, a set of switches, and a "feedback" resistor, which tracks the resistances in the ladder network. A set of binary-weighted currents flows through the "2R" resistors, either to ground, or to a summing bus, as determined by the position of the CMOS switches, operated by the logic inputs from the counter. For example, if the input to S1 is "1", and all the other switches are "0", a current equal to $\frac{1}{2}(E_O/R_O)$ flows through the summing node to match the input current $(-E_1/R_O)$, and the output voltage E_O must be $-2E_1$. If S1 & S2 are "1", with everything else "0", the feedback current is $(3/4)(E_O/R_O)$, and the output voltage, E_O, must be $-(4/3)E_1$.

Since the above two examples occur when the count is $N_{max}/2$ and $(3/4)N_{max}$, the times at which they occur are $T_{max}/2$ and $(3/4)T_{max}$. Similarly, for any other values of N, the gain of amplifier circuit A2 is *inversely* proportional to N (and thus to $T = N\Delta T$). Since the output of the integrator is *directly* proportional to T and the average value of V_{IN} for the interval, T, their product, E_O, is proportional to $\overline{V_{IN}}$ only (Eq. 1).

The integrator must not be allowed to saturate for the worst-case time (T_{max}) and input voltage ($\overline{V_{IN}}_{max}$). At T_{max}, the gain of the A2 circuit is $1/(1 - 2^{-n}) \cong 1$; at that time, the integrator output should be less than or equal to an arbitrary limiting value, V_{LIM}, below saturation:

$$|E_1| = \frac{1}{RC}\,\overline{V_{IN}}\,T_{max} \leq V_{LIM} \qquad (2)$$

Therefore,

$$RC \geq T_{max}\left[\frac{\overline{V_{IN}}_{max}}{V_{LIM}}\right] \qquad (3)$$

$\overline{V_{IN}}_{max}$ can actually be greater than V_{LIM}, if RC is scaled properly. Since T_{max} is also equal to $N_{max}\Delta T$, and $N_{max} = 2^n$ (= 4096 for the AD7521), the clock frequency, $1/\Delta T$, is $2^n/T_{max}$.

A moderate filter capacitance between the output and the summing-point of A2 will reduce switching transients as the gain is switched. A sample-hold following A2 will reduce "ripple" due to the continuing integration between counts (this ripple becomes very small as T_{max} is approached); the new sample should be taken immediately after switching-transients die out. Integrator drift due to offset and bias current in A1 will show up as output offset, reducible by amplifier choice and/or offset trimming with grounded input. Scale-factor errors can be trimmed by adjusting R. Overall accuracy, which improves towards the 0.1% level as T approaches T_{max}, can be well within 1% for $T > 0.1T_{max}$.

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[1] The circuit described here was developed by the author at Industrial Nucleonics Corporation, Columbus OH 43202.

*Use the reply card to request technical data on the AD7520 & AD7521.

RESISTANCE-RATIO-TO-DIGITAL CONVERSION

AD7570 Monolithic CMOS A/D Converter Can Be Used for Tenths-of-a-Percent Resistance Measurements at Low Cost

by Jerry Whitmore

The AD7570* A/D converter, introduced in the last issue of this Journal, has many uses in standard 10-bit conversion applications. Of especial interest for microprocessor applications are the tri-state output logic and "byte-size" enabling logic. However, its analog flexibility, achieved through a design that permits the use of external reference and comparator functions, makes possible an interesting variety of applications. In this Brief, we will consider some resistance-measurement functions.

RESISTANCE DEVIATION

Figure 1 shows a basic configuration in which the AD7570 is used to measure the deviation of an unknown resistance from a standard and convert it to offset binary. The measurement accuracy is independent of the reference-voltage accuracy, since the measurement is performed ratiometrically.

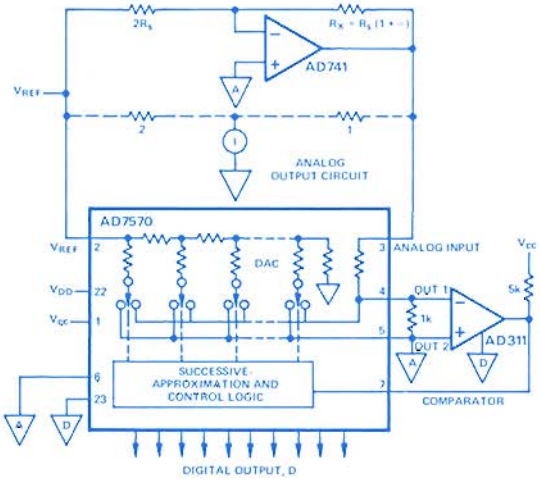


Figure 1. Resistance deviation measurement with binary output, using AD7570 a/d converter. Digital and "housekeeping" circuitry omitted for clarity.

A standard resistance, which is twice the nominal value of the unknown, is the input resistor of an inverter, and the unknown is connected as the feedback resistor. The resistance of the unknown can be expressed as $R_S\ (1 + \alpha)$, where α is the fractional deviation from the nominal resistance, R_S. The output of the inverter is

$$E_1 = -\frac{R_X}{2R_S} V_{REF} = -\frac{V_{REF}}{2}(1+\alpha) \qquad (1)$$

The digital output of the A/D converter will be a fractional binary number between 0 and $(1 - 2^{-10})$ of full-scale, representing the ratio,

$$D = \tfrac{1}{2}(1 + \alpha) = \tfrac{1}{2} + \tfrac{1}{2}\alpha \qquad (2)$$

If $\alpha = 0$, the digital output number will be 10000 00000 = ½; if $\alpha = +\tfrac{1}{2}$, the digital output number will be 11000 00000 = ¾; and if $\alpha = -\tfrac{1}{2}$, the digital output number will be 01000 00000. It is readily seen that these values correspond to an offset-binary code that reads α directly as a bipolar number. If the MSB is complemented, the output reading will be in 2's complement coding – for $\alpha = 0, \tfrac{1}{2}, -\tfrac{1}{2}$, the codes are 00000 00000, 01000 00000, and 11000 00000, irrespective of the value of V_{REF}.

Analog readout may also be provided in the conventional way, by the use of a precision resistance half-bridge, shown in dashed lines. The "null-meter" may be replaced by an op amp for amplification of the null signal. For digital readout with greatly-increased sensitivity, a converter may be connected in the standard bipolar-conversion configuration, to read this amplified error directly with high sensitivity.

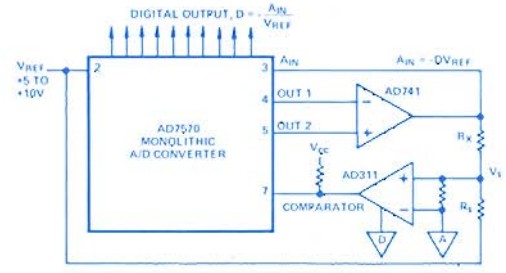


Figure 2. Direct resistance measurement. Digital output is equal to the ratio of R_X to R_S, independently of V_{REF}.

DIRECT RESISTANCE MEASUREMENT[1]

Figure 2 shows a basic configuration in which the analog output of the D/A converter (in the successive-approximations AD7570) is converted to voltage proportional to the digital number, $-DV_{REF}$. This voltage is applied as the A/D converter input. It and the reference voltage are applied to R_X and R_S in series. The comparator acts like an op amp; that is, through the successive-approximation process, it forces the digital number, D, to be whatever value will bring the summing-point voltage, V_S, to within 1 least-significant bit of ground. Thus, at balance, with $V_S \cong 0$,

$$\frac{DV_{REF}}{R_X} = \frac{V_{REF}}{R_S} \qquad (3)$$

and

$$D = \frac{R_X}{R_S} \qquad (4)$$

irrespective of V_{REF}. This scheme can be used to measure any value of R_X less than R_S to within 1LSB of 10 bits, or 1 part in 1024 of R_S, i.e., if $R_S = 10k\Omega$, R_X may be any value from 10Ω to 9,990Ω, measured with a resolution of 10Ω. The voltage, $-DV_{REF}$, may be used as an analog output. ▶▶▶

*Use the reply card for information on the monolithic AD7570.

[1] See also, "Simple A/D Converter Circuit Measures Resistance Digitally", by J. Whitmore, *Electronics*, Oct. 2, 1975.

MEASURE RMS WITH LESS RIPPLE IN LESS TIME

Follow an RMS Converter with a Two-Pole Filter; Design Guides Simplify Component Choice

by Lew Counts

The output of rms-to-dc converters, such as Analog Devices models 440 and 441*, consists of a dc level and an undesired ac "ripple" voltage. The ripple amplitude is inversely proportional to the product of the input-signal frequency and the filter time constant, viz.,

$$\rho \approx \frac{16}{f\tau}, \qquad f > 1/\tau \qquad (1)$$

for sine-wave input, where

- ρ = peak-to-peak ripple voltage as a % of dc output
- τ = 50(ms/μF)C_1 for 440 or 441
- C_1 = 0.2μF + C_{EXT}μF (C_{EXT} an external capacitor)
- f = Input frequency, in Hz

The ripple introduces a small dc error into the rms computation. However, the ripple itself is the limiting uncertainty factor in measuring the rms of low-frequency signals, since the associated dc error is less than 0.1% of reading for values of ρ up to 10%.

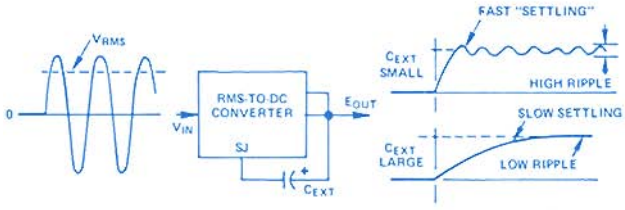


Figure 1. The dilemma — settling time and low-frequency ripple are inversely related for a given choice of C_{EXT}.

Reducing the ripple within the rms converter by adding external capacitance in parallel with the internal filtering capacitor poses a dilemma, illustrated in Figure 1. If the averaging time-constant, τ, is increased, the ripple is reduced; but the settling time to <1% of a step change of input rms is increased in direct proportion to τ,

$$t_{si} \text{ (increasing rms input)} = 2\tau \qquad (2)$$

$$t_{sd} \text{ (decreasing rms input)} = 4.6\tau \qquad (3)$$

The circuit designer can resolve the dilemma by using an external post-filter, like that shown in Figure 2. Here, the two-pole, low-pass filter greatly attenuates the ripple, with only a 40% increase in settling time, for a fixed τ. Or, for the same amount of ripple, the settling time can be greatly decreased. The filter time-constants chosen for the example of Figure 2 provide a critically-damped response to step changes in the input rms level.

Figure 3 graphically compares the ripple for Figures 1 and 2, in the case where C_{EXT} for both is 1μF. Percent ripple, ρ, is plotted as a function of frequency. Note the dramatic reduction of ripple for Figure 2 — the frequencies at which 0.1% and 1% ripple occur are reduced by factors of about 80 and 20, respectively! Figure 3 also shows the ripple-induced dc error in this case, as a function of input frequency; it is negligible, compared to the ripple, in both circuits.

*Use the reply card to request information on models 440 & 441.

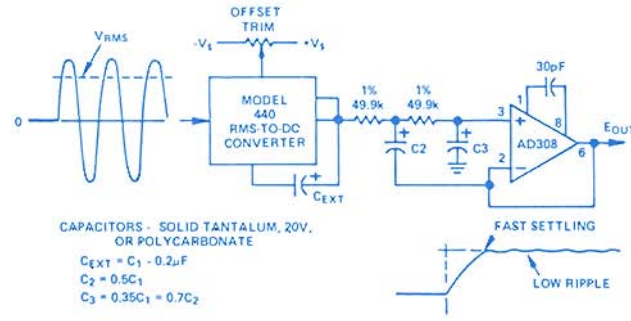


Figure 2. Using an external 2-pole filter to reduce ripple and response time. The text shows how to determine the capacitance, C_1.

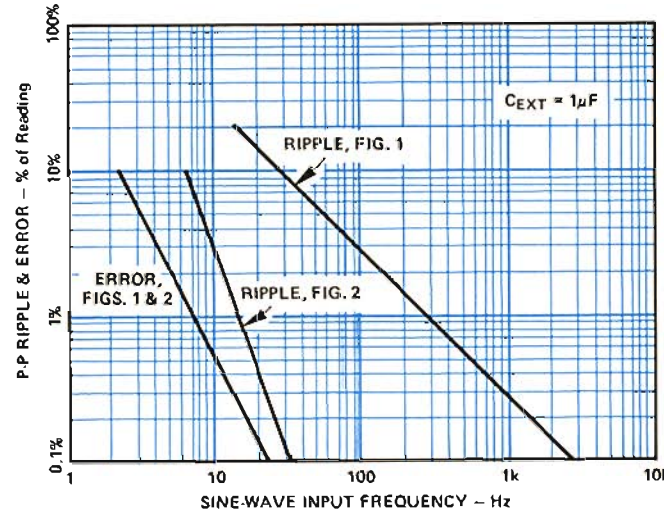


Figure 3. Ripple and error of the 440 and 441 rms-to-dc converters for C_{EXT} = 1.0μF in Figures 1 and 2.

DESIGNING FOR LOW RIPPLE

Figures 4 and 5 make it easy to determine the capacitance values and settling time to <1%, for a desired percentage ripple and a given lower input-frequency, f_L. These curves can be applied directly to designs for symmetrical input signals with crest factors less then 2, such as pure or distorted sine waves, triangular waves, or square waves. The same circuit is also very effective with higher-crest-factor signals (C.F. from 2 to 10), such as pulse trains, if the capacitance values are increased by a factor of 8.

Here is the design procedure:

1. Determine the lowest frequency, f_L, (reciprocal of the longest period) for which the rms converter must filter to 1% or 0.1% ripple.

2. Referring to Figure 4, find the value of capacitance C_1 as the ordinate corresponding to the intersection of f_L and the 1% or 0.1% ripple lines for Figure 2. (Data for Figure 1 is also included for the sake of comparison.)

3. Referring to Figure 2, calculate the values of C_{EXT}, C_2, and C_3.

4. To find the settling time to <1%, use f_L corresponding to 1% ripple for the chosen C_1, and consult Figure 5. Find the value for settling time at the intersection of f_L and each direction of input-rms change (increasing and decreasing).

Example 1. Let f_L = 10Hz for $\rho < 1\%$ p-p ripple (% of reading). Then C_1 = 1.7μF, C_{EXT} = 1.5μF, C_2 = 0.85μF, and C_3 = 0.6μF. The settling times are t_{si} = 0.2s, t_{sd} = 0.4s. By comparison, the circuit of Figure 1 would have $C_{EXT} \cong 30\mu F$, t_{si} = 3s, t_{sd} = 7s for f_L = 10Hz!

Example 2. Let f_L = 20Hz for $\rho < 0.1\%$ p-p ripple. Then, C_1 = 1.7μF, C_{EXT} = 1.5μF, C_2 = 0.85μF, and C_3 = 0.6μF. To determine the settling time to <1%, find f_L for C_1 = 1.7μF and 1% ripple (10Hz), then use Figure 5 to find t_{si} = 0.2s, t_{sd} = 0.4s.

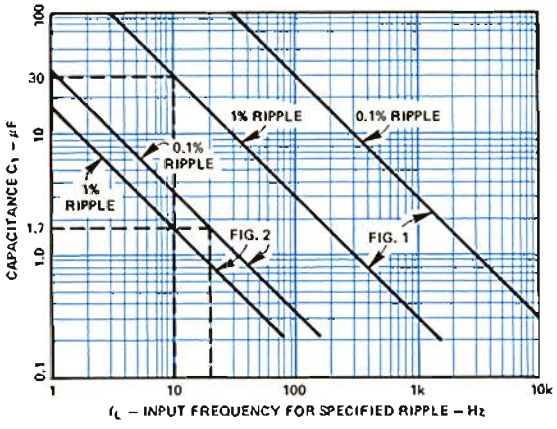


Figure 4. External capacitance (C_1) as a function of f_L, for 0.1% and 1% pk-pk ripple, for both Figure 1 and Figure 2. Dashed lines are for examples in text.

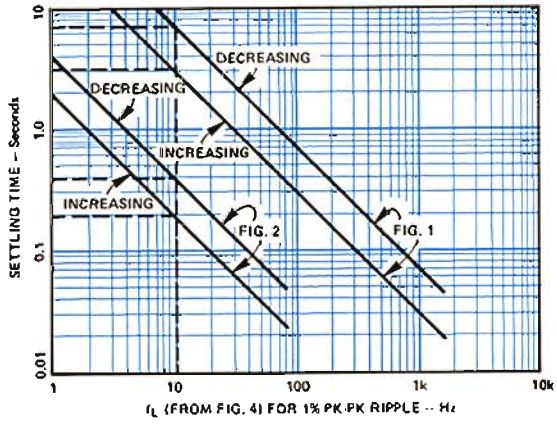


Figure 5. Settling time to 1% of step change of rms for the circuits of Figures 1 and 2, as a function of f_L.

References

Cate, T. and Handler, H. "True-rms Voltage Conversion . . .", *Electronic Design* 4, February 15, 1974.

Sheingold, D. (Editor), *Nonlinear Circuits Handbook*, 1974, Analog Devices, Inc., $5.95.

Potpourri

BRAINSTORMING ON DACs

The term, "digital-to-analog converter" brings to mind computers, data distribution, and general associations to an *output* device that provides a voltage or current that is the final result of a lot of digital manipulation. And properly so!

But, if we look at its circuit (especially that of a simple low-dissipation, essentially passive, monolithic multiplying DAC, such as the AD7520* or the AD7522*), the purely-analog, perhaps audio-oriented engineer can't avoid recognizing that all it "really" is is an attenuator and a set of digitally-operated switches. In other words, a pot with quantized ratios.

As such, if we provide a way of "tweaking" it digitally, we can get precise (or at least, high-resolution), repeatable gain adjustment and linear analog throughput for ac or dc voltages. Since the digital signal can come from an electrically (and perhaps physically) distant location, we can adjust the level of a signal or the value of a reference voltage (e.g., from the high-precision AD2700 10V source* or from the monolithic, low-cost 2.5V AD580*), without marked exposure of the signal to outside interference.

Gain settings can be derived from an automatic digital system (we usually think of it that way), but it can also be programmed *manually* by closing toggle switches or properly-wired thumbwheels. With the AD7522, you can even think about saving wire with a serial input, by dialing or pushing a button in the right coded sequence. You can find useful information on these topics in the *A-D Conversion Handbook*, pp. 1-55 through 1-64.

SAME 440 — TEN TIMES BETTER ACCURACY

When model 440 was first introduced (*Dialogue* 8-1), it had a significant degradation of accuracy when measuring the rms of signals having high crest factors (for example, 2½% error at C.F. = 5). This difficulty in accurately handling complex waveforms with large spike content "bugged" us, since it reduced the utility of a product that was otherwise an excellent value. So, when an improved design became available, with less than 0.15% error at crest factors up to 5, instead of introducing a new model or increasing the price, we quietly incorporated it into all 440's manufactured subsequently and brought the data sheets up to date. *If, as is likely, you haven't known about it, we just thought you might like to know!*

ERRATUM

If you missed the last issue of *Analog Dialogue* (9-2), you also missed the following erratum:

> In the set of illustrations on page 21, facing the article "APPLICATIONS OF THE AD580: The Monolithic Voltage Regulator as a Flexible 3-Terminal Circuit Building Block", the two drawings at the top of the page, under the headings *Precision Reference Source* and *Precision Negative Reference*, have been inadvertently interchanged. Only the circuits themselves have been exchanged; the captions are unaffected.

*For information on these products, use the reply card.

NEW PUBLICATIONS FROM ADI

Short-Form Guide to A/D and D/A Converters is now available. Its 4 pages include specifications and prices on 60 basic A/D and D/A converter types, 8 sample-holds, and the MPX-8A multiplexer. The converters run the gamut of high performance, general purpose, high speed, dual slope, high resolution, ratiometric (A/D) or multiplying (D/A), and high-reliability modules, and include integrated-circuit types, both CMOS and bipolar. **To receive a copy, request "Short-Form Converters".**

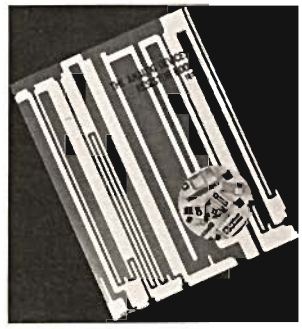
Isolation and Instrumentation Amplifiers is a 16-page brochure describing the application, theory, and selection of single- and multi-channel isolation amplifiers, and instrumentation amplifiers. Specifications and definitions are included. To provide an idea of the range of applicability of the isolators, here is a (reduced) version of a table appearing on page 7:

ISOLATOR SELECTION GUIDE

APPLICATION	PRIMARY CONSIDERATIONS	FEATURES	RECOMMENDED MODEL
Industrial Instrumentation and Control Systems	High Accuracy Low Cost Floating Output	0.05% Max Nonlinearity, 5μV/°C Offset Drift, Adjustable Gain, ±10V Input/Output Range, 3-Port Isolation, Economy	275
Industrial Instrumentation and Control Systems	Highest Accuracy Low Impedance Output	0.03% Max Nonlinearity, 5μV/°C Drift Adjustable Gain, ±10V In/Out, ±5mA Output	285
Industrial Instrumentation and Control Systems	High CMV Adjustable Gain Moderate Accuracy	7.5kV CMV, G = 1 to 100, 0.25% Typical Nonlinearity	274J
ECG/EEG Monitoring	Low Cost Lowest Noise Defibrillator Protection Patient Safety	8μV p-p Noise, 5kV CMV 1.2nA rms Leakage Fixed Gain of 3V/V $49 in 100's	276J (Bipolar)
ECG/EEG Monitoring	Low Noise Patient Safety Defibrillator Protection Low Bias Current	10μV p-p Noise and 5kV CMV (273J) 3μV p-p Noise and 7.5kV CMV (273K) 1.2nA rms Leakage	273J (FET) 273K (FET)
Industrial and Medical Instrumentation	2–200 Channels Low Noise High CMV/CMR	External Synchronization, 14μV p-p Noise, 7.5kV CMV, 115dB Min CMR (5kΩ, 60Hz)	279J
Industrial and Medical Instrumentation	Lowest Cost/Channel 2 or 3 Channels Lowest Noise No Defib. Protection	350V CMV 4μV p-p Noise $48/Channel in 100's (282J) $39/Channel in 100's (283J)	282J, 283J (Bipolar, Open card)
Industrial and Medical Instrumentation	Highest Safety Moderate Noise	7.5kV CMV, 7.5kV Differential 35μV p-p Noise	272J

For your copy of the booklet, request "Diff-Amp Brochure".

The Analog Devices Resistor Book, 1975 is a 16-page guide to thin-film resistance networks. It describes 10 families of general-purpose networks, 12 families of precision ladder networks, and "starter kits". It also provides a guide to specifying user-designed networks. Complete specifications include pricing.



Request "The Resistor Book".

GSA CONTRACTS

Analog Devices, Inc. has been awarded four GSA contracts (General Services Administration, an agency of the U.S. Government) covering: modular power supplies; synchro- and resolver-to-digital and digital-to-synchro and -resolver converters; operational, logarithmic, current, and integrating amplifiers; multipliers; thin-film resistance networks; A/D and D/A converters, and digital panel meters. These contracts make it more convenient for government agencies and certain government contractors to purchase products from ADI. If you are with a U.S. Government agency or subcontractor authorized to purchase on GSA contracts, you can obtain our GSA price list and catalog by writing for it on your official letterhead.

Worth Reading

LAST ISSUE OF *ANALOG DIALOGUE*
Volume 9 (1975), Number 2

If you haven't seen the last issue of *Dialogue*, you can get a copy by requesting it. Here's what you've missed:

Editor's Notes, Authors
10-Bit Monolithic CMOS A/D Converter (AD7570)
Root Mean-Square Digital Panel Meter for True RMS (AD2011)
An Improved 12-Bit Multiplying D/A Converter (DAC1125)
Isolation Amplifiers for Effective Data Acquisition
New Products:
- Compact, Low-Cost 12-Bit A/D Converter (ADC1133)
- Low-Cost Line-Powered 3½-Digit Panel Meter (AD2009)
- Instrumentation Amplifier with Low Drift, Noise, and Cost (Model 610)
- 2.5V Monolithic Voltage Reference with 10ppm/°C (AD580M)
- Thin-Film Resistance-Network "Starter" Kits (AD1890)
- High-Accuracy 10V Hybrid Reference Supply (AD2700)
- Precision Comparators: AD111/211/311
- Monolithic 8-Bit DAC is High-Performance, Low-Cost Alternative to 1408-1508 (AD559)
- 12-Bit Integrated-Circuit DAC Includes Precision Reference (AD563)

Application Briefs:
- *Automatic Gain Measurement Using D/A Converters*
- *Two-Speed Synchro Conversion Systems*
- *Applications of the AD580 2.5V 3-Terminal Reference*

Potpourri: An Application Quickie on the AD562, More Authors
Worth Reading: Last Issue of *Dialogue*, Book Review, Errata
Advertisements: IC DAC's and FET's

BOOKS RECEIVED

The titles mentioned here are generally relevant to the fields we serve and are published here for the information of our readers. Their appearance in this column is not an endorsement by *Analog Dialogue*, and they are *not* available from Analog Devices.

The Bugbook III, Microcomputer Interfacing, by David G. Larsen, Peter R. Rony, Jonathan A. Titus, paperback, E & L Instruments, Inc., Derby, Connecticut 06418, 1975.

Operational Amplifiers, Theory and Practice, by James K. Roberge, 659 pp., xvii, John Wiley & Sons, Inc., New York, 1975.

Operational Amplifiers, Theory and Servicing, by Edward Bannon, 195 pp., x, Reston Publishing Co., Inc., Reston, Virginia, 1975.

Unique IC Op-Amp Applications, by Walter G. Jung, paperback, 144 pp., Howard W. Sams & Co., Inc., Indianapolis, 1975 (Extracted from *IC OP-Amp Cookbook* (see *Dialogue* 9-2.))

Audio Op-Amp Applications, by Walter G. Jung, paperback, 144 pp., Howard W. Sams & Co., Inc., Indianapolis, Indiana, 1975, see above item.

Handbook of Integrated-Circuit Operational Amplifiers, by George B. Rutkowski, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 321 pp., x, 1975.

THE REASON YOU'LL ALWAYS NEED OUR MODULAR CONVERTERS IS THIS SIMPLE.

There's a lot happening in integrated circuits nowadays. And frankly, when it comes to linear ICs, we're the people who are making it happen. So whenever we introduce a new IC, our modules are the first to know.

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They use our hot new 12-bit IC DAC, the AD562. So both our new modules are much smaller and much less expensive than their predecessors—two-thirds the price and only half the size, with no trade-off on performance.

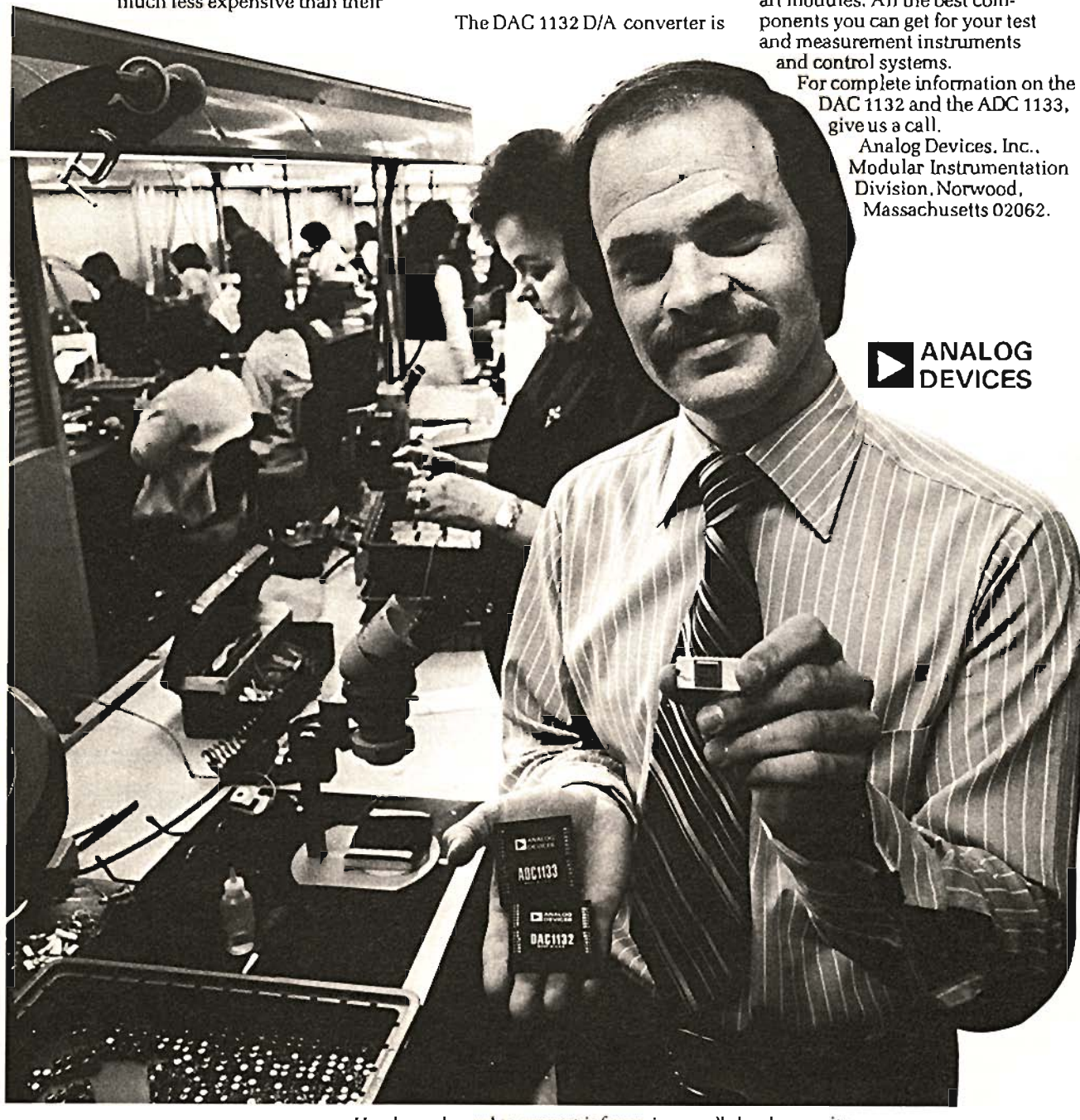
The ADC 1133 packs the performance of much larger, more expensive A/D converters into a 2 x 2 x .4-inch module. You get true 12-bit accuracy, 25 μsec speed, and a very low gain temperature coefficient—8ppm/°C. It's the first time you've ever been able to get this kind of performance in such a small package.

The DAC 1132 D/A converter is also only 2 x 2 x .4-inches. It includes our high-performance IC, plus an input storage register, output amp, and precision voltage reference source. And it delivers a fast 2 μsec settling time and the same low (8ppm/°C) gain TC as the 1133.

Two new modules, made possible by the AD562. And there's more to come. More new state-of-the-art ICs. More new state-of-the-art modules. All the best components you can get for your test and measurement instruments and control systems.

For complete information on the DAC 1132 and the ADC 1133, give us a call.

Analog Devices, Inc., Modular Instrumentation Division, Norwood, Massachusetts 02062.



ANALOG DEVICES

Use the reply card to request information on all the above units.